SINGER
INSTRUMENTATION

SIGNAL GENERATOR

MODEL 6201

INSTRUCTION MANUAL NO. 110-5103

MP MASTER
MA30333

INSTRUCTION MANUAL

SIGNAL GENERATOR

MODEL 6201

INSTRUCTION MANUAL NO. 110-5103

SINGER
INSTRUMENTATION

The Singer Company, Palo Alto Operation

3176 Porter Drive, Palo Alto, California 94304 / (415) 493-3231 TWX 910-373-1765

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Instruments should be returned only on prior written authorization from the Singer Representative or the factory(1). Please provide the following information in order to expedite our processing of your instrument:

1. Model or Type
2. Serial Number
3. Approximate date instrument was placed in operation
4. Approximate number of hours of use
5. Description of trouble(2)
6. Has maintenance action been previously requested?
7. Other comments

Upon receipt of this information our Service Department will send you service data or shipping instructions. Upon receipt of shipping instructions forward the instrument prepaid to the specified center or factory. If requested, an estimate of charges will be made before work begins.

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(2) Include data on symptoms, measurements taken, test instruments used, suspected location of trouble, maintenance action taken, and any other relevant data.

MANUAL CHANGES

FOR

6201

Make changes and additions as indicated below:

CHANGE 1: Schematic 106-0808-001 and Parts List, Assembly A3A1;

A. Change the value of C22 from .0047 μF to "FACTORY SELECT".

B. Change the value of C16 from 100 pF to 30 pF, ±2%, 500 V, 150-2002-300EGO, 72136, DM15E300GO.

CHANGE 2: Schematic 106-0808-001 and Parts List, Assembly A3A2A1;

A. Change the Singer Parts No. of L4 from 132-0380-001 to 132-0380-004.

B. Change the Singer Parts Nos. of Q1, Q2 from 153-3032-001 to 153-3032-002.

CHANGE 3: Schematic 106-0788-001 and Parts List, Assembly A4A1;

A. Add C76, 1 pF, ±0.1 pF, 50 V, fixed cer., 150-7002-003, 29990, 100-A-1R0-B-C-50.

B. Add R43, 15 Ω, ±10%, 0.10 W, fixed cer., 151-6000-150, 14298, CRC-20-15Ω.

C. On schematic, connect C76, 1 pF to conector of Q7, in series with R48, 15 Ω, to ground.

D. On schematic, change Q7 from RE3754 to D5E.

These changes do not apply to all units, but the D5E transistor requires addition of C76 and R43.

CHANGE 4: Schematic 106-0784-001 and Parts List, Assembly A7;

A. Change the value of R24 from 31.6 KΩ to 21.5 KΩ, ±1%, 1/4 W, fixed MF, 59-21.5K, 19701, MF5C-D-2152F.

B. Delete * from R89 and R59.

C. Add * to R33.

D. Change the value of R59 from 38.3 KΩ to 34.8 KΩ (FACTORY SELECT).

E. Add (FACTORY SELECT) after the value of R33.

F. Change R89 from "FACTORY SELECT" to 20.0 KΩ (FACTORY SELECT).

G. For schematic in upper right hand corner change Pin 5 to read Pin 6. Put wire shielding symbols on wire leading to Pin 9, Pin 8 and Pin 6.

CHANGE 5: Schematic 106-0773-001 and Parts List, Assembly A8A3A6;

A. Change the value of R26 from 560 Ω to 1 KΩ, 151-1002-102J, 19701, CR25-1-4-5P-1K.

B. Change the value of C16 from .01 μF, 150 V to .01 μF, 50 V, 12-88, 8121-100-W5R-103K.

CHANGE 6: Schematic 106-0789-001 and Parts List, Assembly A9A1; change the true mfg. part no. from W005 to 1N4005.

CHANGE 7: Schematic 106-0792-001 and Parts List, Assembly A9A2;

A. Change the Singers Part No. of A9A2 from 103-3028-004 to 103-3028-001.

B. Change Singers Part No. for CR1 from 154-2002-001 to 81-269.

C. Change Singers Part No. for Q11 from 153-3028-001 to 81-140.

D. Change the value of R15, R20 from 1.0 Ω to 0.5 Ω, ±5%, 2.5 W, 151-2029-001, 91637, RS2C-.5Ω-5%.

E. Change the value of R27 from .36 Ω to 0.17 Ω, ±5%, 5 W, 151-2029-001, 91637, RS-5-.17Ω-5%.

Apply part list changes to schematic.

CHANGE 8: Schematic 106-0853-001 and Part List, Assembly A7A2; change Pin J-P1 Meter Ckt (30%) to (15%) and Terminal M-P1 from $\overline{k_1 k_2}$ to $k_1 \overline{k_2}$.

CHANGE 9: Schematic 106-0809-001 and Parts List, Assembly A13; change one word from "Remote" to "Operate" at terminal R.

ECO #15161, #15186, #15205, #15214, #15215, #15217, #15220, #15237, #15263.

April 5, 1974

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Figure 1-1. Model 6201 Signal Generator

SECTION I
GENERAL INFORMATION

1–1. GENERAL DESCRIPTION.

1-2. The Model 6201 Signal Generator (Figure 1-1) hereinafter referred to as the Signal Generator, is a general purpose, high performance RF signal generator that provides exact frequency tuning from 7.75 MHz to 512 MHz in six over-lapping bands. This wide frequency range is obtained by dividing down the basic frequency of a tunable, solid-state master oscillator (248 to 512 MHz), using a binary frequency-divider network arrangement. The divider output is then amplified, filtered and attenuated (as appropriate) to provide RF output level of from +20 dBm (2.2 volts) to -146 dBm (0.11 microvolt) into 50 ohms. As internal leveling circuit maintains the RF output level flat within ±0.25 dB up to 125 MHz; and within ±0.5 dB from 125 MHz to 512 MHz.

1-3. The divider output is also coupled to a frequency counter that in turn, drives a six-digit front panel frequency readout display and a digital frequency locking circuit which maintains the precise stability of the master oscillator. Through the use of a unique digital frequency-locking circuit, the accuracy of the RF output is maintained between 0.00032% and 0.0016% depending on the frequency band selected. The counter, which provides direct readout of the selected frequency, may also be used to measure external signals within the frequency range of 100 Hz to 10 MHz.

1-4. Modulation capabilities include amplitude modulation (AM), frequency modulation (FM), and pulse modulation (PM), with a total capability of providing simultaneous AM/FM or FM/PM using internal or external modulation modes, or a combination of both.

1–5. PURPOSE AND USE OF EQUIPMENT.

1-6. The Signal Generator with its wide frequency range, flat response, frequency stability and resolution, wide range of output signal levels, and versatile modulation capabilities provides an excellent instrument for performing electronic equipment tests which include the following:

a. Evaluating modulation techniques and receiver performance with AM, FM, pulse, AM/FM, FM/pulse or FM signals.

b. Aligning and testing of AM, FM and radar receivers.

c. High-level testing of amplifiers, mixers, multipliers, etc.

d. Testing sensitive narrowband receivers.

e. Accurate, stable measurement of attenuators.

f. Measuring dynamic AM rejection in AM/FM systems.

g. Doppler-shift moving target signal simulation.

h. Ratio detector/discriminator alignment.

i. Measuring limiter time constant.

j. Narrowband component analysis.

k. Multipole filter response characteristics.

l. Determining receiver signal-to-noise ratio.

1–7. SPECIFICATIONS.

1-8. The electrical and physical characteristics of the Signal Generator are listed in Table 1-1.

1–9. EQUIPMENT SUPPLIED.

1-10. The Signal Generator is shipped complete and is ready for use upon receipt. The complete Signal Generator consists of the following items:

a. One (1) Model 6201 RF Signal Generator (Singer part number 101-0452-003).

b. One (1) line cord (Singer part number 180-0001-001).

c. One (1) panel cover (Singer part number 103-1982-001). Not shipped if accessory plug-in module is ordered with Signal Generator.

1–11. ACCESSORIES AND OPTIONS.

1-12. The accessories and options that are available for use with the Signal Generator are listed in Table 1-2. The accessories and options are supplied only when specifically ordered.

TABLE 1-1. SPECIFICATIONS

Parameter	Specification
FREQUENCY CHARACTERISTICS	
Frequency Range:	7.75 - 512 MHz in six bands: Band 1: 248 MHz - 512 MHz Band 2: 124 MHz - 256 MHz Band 3: 62 MHz - 128 MHz Band 4: 31 MHz - 64 MHz Band 5: 15.5 MHz - 32 MHz Band 6: 7.75 MHz - 16 MHz
Frequency Vernier Range:	> 300 ppm
Frequency Resolution:	Continuously tunable. Six digit frequency display with a least significant digit of 100 Hz (7.75 - 62 MHz) or 1 kHz (62 - 512 MHz).
Frequency Accuracy:	
Locked mode:	±(0.05 of last digit + time base accuracy).
Unlocked mode:	±(last digit + time base accuracy).
Time Base Accuracy:	
Standard:	< ±1 ppm after two hour warm up @ 25°C.
Option:	< ±0.1 ppm after two hour warm up @ 25°C.

Frequency Stability:	Locked	Unlocked
Time (after two hr. warm up):	< 1 ppm/24 hrs.	< 10 ppm/10 mins.
Temperature (0°C to 55°C):	<0.33 ppm/°C (Option: 0.03 ppm/°C)	< 60 ppm/°C
Line Voltage (±10% change):	< 1 ppm	< 10 ppm
Load (open to short):	None	None
Level change:		
10 dB vernier	None	1 ppm
10 dB steps	None	None
Mode change:		
CW to AM	None	None
CW to FM	*	< 150 ppm of carrier frequency

Frequency lock hold range:	±600 ppm or ±10°C min.
SPECTRAL PURITY CHARACTERISTICS	

Residual FM:	Mode	CW		FM Up to max. Pk. Dev.	
	Post Detection Bandwidth	300 Hz - 3 kHz	20 Hz - 15 kHz	300 Hz - 3 kHz	20 Hz - 15 kHz
	248 - 512 MHz	< 5 Hz	< 15 Hz	< 9 Hz	< 30 Hz
	124 - 256 MHz	< 3 Hz	< 7 Hz	< 5 Hz	< 15 Hz
	7.75 - 126 MHz	< 2 Hz	< 5 Hz	< 3 Hz	< 8 Hz

* Not discernible at modulation frequency $\geq$ 1 kHz, increasing to < 1% peak deviation at 100 Hz modulation frequency.

TABLE 1-1. SPECIFICATIONS (CONTINUED)

Parameter	Specification
SPECTRAL PURITY CHARACTERISTICS (Continued)	
Spurious Signals:	
Harmonics:	> 30 dB below carrier
Sub-Harmonics:	> 45 dB below carrier
Non-Harmonics:	Not perceptible
Broadband Noise:	130 dB below carrier in a 1 Hz bandwidth at maximum power level vernier position over entire frequency range.
RF POWER OUTPUT CHARACTERISTICS	
Output Power Control Range:	20 dBm (2.2 V) to -146 dBm (0.01 μV) in 10 dB steps with continuous adjustment between steps. Output level indicated on attenuator and meter calibrated in dBm and volts into nominal 50 Ω load.
RF Output Level Accuracy:	

Output Level Range:	+20 dBm to -10 dBm	-10 dBm to -50 dBm	-50 dBm to -146 dBm
Total inaccuracy as indicated on output meter and step attenuator (including flatness, calib. inaccuracy, attenuator inaccuracy, meter linearity, detector response, etc.)	Up to 125 MHz ±1.0 dB	Up to 125 MHz ±1.5 dB	Up to 125 MHz ±2.2dB
	Up to 512 MHz ±1.2 dB	Up to 512 MHz ±1.8 dB	Up to 512 MHz ±2.5 dB

Auxiliary Accuracy Specifications:	
Attenuator Accuracy:	±0.15 dB/10 dB cumulative. Up to ±1.5 dB max.
RF Level Flatness:	Up to 125 MHz: ±0.25 dB Up to 512 MHz: ±0.5 dB
Meter Linearity:	±2% of full scale.
Output Impedance:	50 Ω nominal.
Output VSWR	< 1.25 @ ≤ 0 dBm; <1.5 @ > 0 dBm
Output Connector:	Type N Female.
MODULATION CHARACTERISTICS	
Internal AM:	
Frequency:	1 kHz screw driver adjustable ±2% (rear panel).
Range:	Zero to 100% indicated on AM meter calibrated in % modulation.
Accuracy of Indicated AM:	±8% of reading (20% - 100%) over top 3 dB of vernier range. ±16% of reading (20% - 100%) over remaining 7 dB of vernier range.
Incidental FM - Up to 125 MHz: (30% AM)	< 150 Hz peak
Up to 512 MHz:	< 300 Hz peak
AM Distortion: (over top 3 dB of vernier range)	< 5% up to 70% AM fc < 250 MHz < 3% up to 30% AM fc > 250 MHz < 10% up to 70% AM fc > 250 MHz

TABLE 1-1. SPECIFICATIONS (CONTINUED)

Parameter	Specification
MODULATION CHARACTERISTICS (Continued)	
External AM: [1]	
Modulation Frequency Response: [2]	DC to 100 kHz @ 30% AM
Sensitivity:	< 2 volts RMS for 95% AM
Accuracy of Indicated AM:	Same as Internal AM. (1 kHz modulation frequency)
AM Distortion:	Same as Internal AM. (Modulation frequency < 5 kHz)
Incidental PM: (30% AM)	< 0.15 radians peak up to 125 MHz. 0.3 radians peak up to 512 MHz.
Incidental FM:	Equal to incidental PM times modulation frequency
Input Impedance:	600 Ω nominal
Input Connector:	BNC, Female
Internal FM:	
Modulation Frequency:	1 kHz screw driver adjustable ±2% (rear panel).
Deviation:	0.1% peak of carrier frequency indicated on meter with full scale ranges of 30, 100, 300 and 1000 kHz peak. Vernier provides continuous control down to zero deviation.
Meter Accuracy:	±5% of full scale
External FM:	
Modulating Frequency Response: [3]	
Unlocked:	DC - 200 kHz
Locked:	100 Hz - 200 kHz
Deviation:	> 0.5% peak of carrier frequency indicated on meter with full scale ranges 30, 100, 300 and 1000 kHz peak. Vernier provides continuous control down to zero deviation.
Sensitivity:	< 2.7 V for maximum deviation. Positive going voltage increases frequency.
Distortion:	< 1% at 0.1% deviation over entire modulation frequency range.
Meter Accuracy:	±5% of full scale up to 0.1% deviation. (50 Hz to 200 kHz)
Incidental AM:	> 50 dB below carrier at ±0.1% deviation.
Input Impedance:	5000 Ω nominal
Input Connector:	BNC, Female
External Pulse Modulation:	
Repetition Rate Range:	10 Hz - 500 kHz
Pulse Level:	Actual RMS value of pulse peak level indicated by front panel meter.

[1] Specifications apply to the top 10 dB range of the output vernier.

[2] Frequency range where the actual % AM deviates less than ±1 dB from the % AM at 1 kHz.

[3] Frequency range where the actual peak deviation deviates less than ±1 dB from the peak deviation at 1 kHz.

TABLE 1-1. SPECIFICATIONS (CONTINUED)

Parameter	Specification
MODULATION CHARACTERISTICS (Continued)	
External Pulse Modulation (Cont.)	
Pulse Level Accuracy:	CW level accuracy plus sample response for pulse width > 4 μsec: < 1 dB.
	Response for pulse width > 10 μsec: < 0.1 dB. (PRf > 50 Hz, duty cycle > 0.1%).
Rise and Fall Time:	Down to 20 nsec, varying with frequency and pulse width.
On/Off Ratio:	60 dB from 7.75 MHz to 150 MHz, decreasing to 45 dB at 512 MHz.
Sensitivity:	< 1 volt turns RF on to level indicated on meter.
Input Connector:	BNC, Female
Input Impedance:	50 Ω nominal
RF Power Off:	Output decreased by on/off ratio when AM PULSE pushbutton is pressed.
COUNTER CHARACTERISTICS (Externally Applied Signal)	
Frequency Range:	100 Hz to 10 MHz
Frequency Resolution:	±1 Hz up to 1 MHz with time base set to 1 sec. ±10 Hz up to 10 MHz with time base set to 0.1 sec. or ±1 Hz with time base set to 1 sec and first digit dropped off.
Count Accuracy:	± last digit plus time base accuracy.
Time Base Accuracy:	
Standard:	±1 ppm after two hours warm up @ 25°C
Option 7:	±0.1 ppm after two hours warm up @ 25°C
Input Waveform:	Sinusoid, trapezoid, or pulse with 50 nsec min. width
Sensitivity:	200 mV rms
Input Impedance:	10,000 Ω nominal
Input Connector:	BNC, Female
OTHER CHARACTERISTICS	
1 kHz Output	> 1 volt peak with 1% distortion Z_{out} = 1000 Ω nominal
External Counter Time Base Frequency Standard Input:	1.00000 MHz (rear panel BNC connector).
Input Impedance:	10 kΩ nominal
Minimum Input Signal Level:	100 mV rms
Dimensions:	5-1/4" high x 16-3/4" wide x 22" depth behind front panel
Weight:	53 pounds
Power:	115 or 230 volts (±10%) 47 to 420 Hz, 60 watts.
Operating Temperature Range:	0° to 55°C

TABLE 1-2. ACCESSORIES AND OPTIONS

Accessories/Options	Purpose
ACCESSORIES	
Model 6202 Range Extender (plug-in module), Singer Part No. 101-0465-001	Extends frequency range of Signal Generator down to 61 kHz.
Model 1024 Frequency Doubler, Singer Part No. 102-0175-001	Extends frequency range of Signal Generator up (one octave) to 1024 MHz.
Rack Mounting (ears) Kit, Singer Part No. 102-0185-001	Provides brackets for mounting Signal Generator in standard 19-inch rack.
Rack Mounting Kit, with slides, Singer Part No. 102-0184-001	Provides brackets, with slides, for mounting Signal Generator in standard 19-inch rack.
OPTIONS	
Programmable RF output power level control	Provides a programmed 8-4-2-1 binary code to step attenuate the RF output from 0 to 150 dBm.
Internal 400 Hz modulation source	Provides 400 Hz internal modulating source in place of standard 1 kHz source.
Rear-panel RF output and modulation input connectors	Provides rear-panel RF OUT and modulation input connectors in place of front-panel connectors.
0.1 ppm counter time base accuracy 0.03 ppm/°C time base temperature stability	Increases time base accuracy of frequency counter and long-term stability of Signal Generator.

SECTION II
OPERATION

2–1. INSTALLATION.

2-2. The Signal Generator is shipped complete and ready to use upon receipt. After the equipment has been unpacked, check the contents of all shipping containers against the packing invoice to ascertain that the order is complete.

2-3. INCOMING INSPECTION.

2-4. Examine the equipment for indications of damage which may have occurred during shipment. Check all front panel controls for freedom of movement, full travel and positive detent locking. Note any evidence indicating that the equipment has sustained a severe mechanical shock.

2-5. POWER REQUIREMENTS, CONNECTION AND TURN-ON.

2-6. The Signal Generator is designed to operate from either a 115 volt or 230 volt (±10%), 47 to 420 Hz power line. Power consumption is approximately 60 watts without optional equipment. To couple the Signal Generator to line power, proceed as directed in the following steps.

CAUTION

The Signal Generator is normally shipped with a line protective fuse rated at 1 ampere (delay type) installed and the rear panel 115 V/230 V slide switch set to the 115 V position. If the Signal Generator is to be powered from a 230 volt line, install a delay type fuse rated at 1/2 ampere @ 230 V in place of the 1 ampere fuse, set the 115 V/230 V slide switch to 230 V and conspicuously mark the Signal Generator to indicate it has been modified for 230 volt operation.

a. Determine the voltage available at the power output receptable. If the line voltage is 230 volts, set the rear panel 115 V/230 V slide switch to the 230 V position and install a delay type fuse rated at 0.5 ampere @ 230 V into the rear panel fuseholder.

b. Couple the female connector of the supplied power cord to the rear panel power input receptacle.

WARNING

The Signal Generator is designed for operation from a polarized three-terminal (one ground) power receptacle. If a three-terminal power receptacle is not available, a three-prong to two-prong adapter should be used to prevent a potential shock hazard. Connect the pigtail lead of the adapter to power receptacle ground.

c. Couple the polarized male connector at the other end of the supplied power cord to the line power receptacle.

d. Press the POWER pushbutton switch; the Signal Generator is now energized and the frequency display readout will light. For maximum stability, allow a warmup period of 30 minutes between application of power and actual use.

2-7. ENVIRONMENT.

2-8. The Signal Generator should be operated in a relatively dust-free environment. There is no fan or unusual ventilation requirement if the ambient temperature is below 55°C.

2-9. BENCH MOUNTING.

2-10. For bench operation, the Signal Generator should be placed on a sturdy, vibration-free surface. The front panel of the instrument can be elevated slightly for easier access to controls and connectors by lowering the tilt stand located underneath the cabinet.

2-11. RACK MOUNTING.

2-12. To install the Signal Generator in a standard 19-inch rack, proceed as directed below.

WARNING

Before installing the Signal Generator into the rack, perform Steps a and b of paragraph 2-6.

a. Remove both decorative side panel plates from the Signal Generator by unscrewing the eight 6-32 screws that secure each panel to the equipment frame.

b. Remove feet and tilt bar from bottom cover of the Signal Generator.

c. Secure the set of rack slides and spacer plates (furnished with rack-mounting kit) to the new side panel plates supplied, using 10-32 panhead screws and nuts with captive lockwashers.

d. Note that the new side panels will fit upsidedown and backwards; fit them so the holes are nearest the bottom of each side. Position the spacer plates so the widely spaced holes (4.12") are to the front, and mount the slides so the fixed flanges (on the slides) are to the front. Be sure the holes in the fixed flanges match those in the rack-mount ears (step g); if not, switch the slides to the opposite side of the panel plates.

e. Mount the adjustable flanges on the back of each slide, with the flange extended away from the side plate.

f. Secure the two side panel plates and slides to the Signal Generator frame, using the eight 6-32 flat-head screws removed in step a.

g. Attach the rack-mount ears to each handle casting with four 8-32 screws supplied.

h. Install the Signal Generator into the rack. Secure the mounting ears to the rack.

i. Perform steps c and d of paragraph 2-6.

2-13. OPERATING CONTROLS, INDICATORS AND CONNECTORS.

2-14. The front-panel operating controls, indicators, and connectors for the Signal Generator are shown in Figure 2-1 and described in Table 2-1. Similarly, the rear-panel controls and connector are shown in Figure 2-2 and described in Table 2-2.

2-15. OPERATING PROCEDURES.

2-16. UNMODULATED (CW) OPERATION.

2-17. To obtain an unmodulated RF output from the Signal Generator, proceed as follows:

a. Press CW pushbutton.

b. Set RANGE MHz selector switch to the desired frequency band.

c. Set VERNIER frequency control to mid-range.

d. Rotate FREQUENCY control until the desired output frequency is approximately indicated on the frequency digital readout display.

e. Rotate VERNIER frequency control until the exact frequency is indicated on the digital readout display. If greater frequency stability is required, momentarily place LOCK/NORMAL switch in LOCK position. The LOCK indicator will light when the frequency lock mode is established.

f. Couple the RF OUTPUT connector to the load (ideally, a nominal 50 Ω load) via a 50 ohm cable.

CAUTION

To prevent damage to the Signal Generator, do not connect to a load that will supply AC or DC current back into the Signal Generator output.

NOTE

Coupling the RF OUTPUT connector to a mismatched load may not affect the RF LEVEL meter indication, but the RF LEVEL meter will not indicate the true voltage appearing across the load. To calculate voltage across a load other than 50 Ω, consider the Signal Generator as a ideal voltage source of value 2E behind 50 Ω where E is the output voltage indicated by the RF LEVEL meter. The voltage across the load is:

$$V_L = 2E \frac{R_L}{R_L + 50}$$

g. Set the dBm step control and associated vernier control to obtain the desired RF output power or voltage level on RF LEVEL meter (see examples).

EXAMPLES

1. Desired output power level is -47 dBm. Set the dBm switch (outer concentric control) to -40/3 mV; and adjust the dBm vernier control (inner concentric control) to obtain an RF LEVEL meter indication of -7 on the dB scale.

2. Desired output voltage level is 200 μV. Set the dBm selector switch to -60/0.3 mV; and adjust the dBm vernier control to obtain an RF LEVEL meter indication of 0.2 on the lower VOLTS scale.

h. To increase the RF output power level by 6 dB or the RF output voltage level by a factor of 2, press Vx2 pushbutton.

2-18. INTERNAL AM OPERATION.

2-19. To obtain an amplitude-modulated RF output using the internal 1 kHz oscillator, proceed as follows:

a. Obtain an unmodulated RF output (refer to paragraph 2-16).

NOTE

For linear amplitude modulation, always maintain the Vx2 pushbutton in the released position during AM operation.

b. Rotate the AM LEVEL control fully counterclockwise, and press the AM INT pushbutton.

NOTE

When AM INT pushbutton is pressed, the internal 1 kHz oscillator signal (1.5 volt peak-to-peak) is available at the front-panel 1 kHz MOD OUT connector (source impedance: 1000 ohms).

c. Set the AM/FM switch to AM.

d. Adjust the AM LEVEL control until the desired percentage of amplitude modulation is indicated on the % AM scale of the % AM/FM DEV meter.

2-20. EXTERNAL AM OPERATION

2-21. To obtain an amplitude-modulated RF output using an external DC to 200 kHz signal, proceed as follows:

TABLE 2-1. FRONT-PANEL OPERATING CONTROLS, INDICATORS AND CONNECTORS

Index No. (Figure 2-1)	Control, Indicator or Connector	Function
1	% AM/FM DEV meter	Indicates percentage of amplitude modulation on one scale (0 to 100%) or peak deviation of frequency modulation on two scales (0 to 30 or 0 to 100). Meter mode and FM scale are selected by AM/FM switch (2) and FM RANGE kHz pushbuttons (15), respectively.
2	AM/FM switch	Selects either percentage of amplitude modulation or FM peak deviation for readout on the % AM/FM DEV meter.
3	FM DEV control	Adjusts the peak deviation sensitivity in both internal and external FM modes. Clockwise rotation increases the peak deviation. The control is used after the FM meter and peak deviation circuitry are properly calibrated by the FM CAL control (14).
4	RANGE MHz switch	Selects desired frequency octave band as follows: Band 1: 248 MHz to 512 MHz Band 2: 124 MHz to 256 MHz Band 3: 62 MHz to 128 MHz Band 4: 31 MHz to 64 MHz Band 5: 15.5 MHz to 32 MHz Band 6: 7.75 MHz to 16 MHz **NOTE** When the RANGE MHz selector is set to the PLUG-IN position, the frequency octave band is determined by the setting of the plug-in frequency extender module (if used).
5	Frequency display readout	Provides a six-digit readout display of either the RF output frequency of Signal Generator or an external 100 Hz to 10 MHz signal.
6	FREQUENCY control	Provides continuous adjustment of the output frequency over any selected octave band.
7	RF LEVEL meter	Indicates RF output power and voltage at RF OUT connector, when Signal Generator is properly terminated by a 50 ohm load. The output level, in dBm, is equal to the algebraic sum of the meter dB scale reading and the dBm step selector (9) setting (plus 6 dB if Vx2 pushbutton is pressed). The output voltage is equal to the appropriate meter VOLTS scale reading and scale factor (times 2 if Vx2 pushbutton is pressed).
8	Vx2 pushbutton	When pressed, increases RF output voltage by a factor of 2 and RF output power by 6 dB.
9	POWER pushbutton	When pressed, applies AC line power to the Signal Generator.
10	dBm controls:	
	Step selector switch (outer concentric control)	Attenuates RF output signal from 0 to 150 dB, in 10 dB steps.
	Vernier control (inner concentric control)	Provides continuous RF level adjustment over a 12 dB range (nominal). The combination of the dBm step control and vernier control provide for continuous RF output level adjustment from +20 to -146 dBm.

TABLE 2-1. FRONT-PANEL OPERATING CONTROLS, INDICATORS AND CONNECTORS (CONTINUED)

Index No. (Figure 2-1)	Control, Indicator or Connector	Function
11	RF OUT connector	Type N female connector (Z_o = 50Ω) which provides RF output of Signal Generator.
12	VERNIER frequency control	Provides fine adjustment of the output frequency.
13	LOCK/NORMAL switch and indicator	When switch is momentarily placed in LOCK position, causes RF output frequency to be locked to stable reference of frequency counter, thereby achieving a stability of 1 ppm/24 hours. NORMAL position maintains the standard frequency stability. Indicator goes on when the Signal Generator is in the frequency lock mode.
14	FM CAL push-to-operate controls	Used to calibrate the amount of FM deviation in both internal and external FM modes.
15	FM RANGE (kHz) pushbuttons	Permit selection of any one of four FM deviation sensitivity ranges (30 kHz, 100 kHz, 300 kHz or 1000 kHz) when the % AM/FM switch is set to FM.
16	FM connector	BNC connector for coupling external signals to frequency modulate the RF output, when FM EXT pushbutton (18) is pressed.
17	1 kHz MOD OUT connector	BNC connector which provides a 1 kHz sinewave output from the Signal Generator during internal FM or internal AM operation.
18	FM pushbuttons:	
	INT pushbutton	When pressed, allows internal 1 kHz signal to frequency modulate the RF output.
	EXT pushbutton	When pressed, allows external signals coupled to FM, connector (16) to frequency modulate the RF output.
19	AM/PULSE connector	BNC connector for coupling external sinusoidal or pulse signals to amplitude modulate the RF output, when AM EXT pushbutton or AM PULSE pushbutton, respectively, is pressed.
20	EXT COUNT pushbutton and connector	When pushbutton is pressed, allows an external 100 Hz to 10 MHz signal at the associated BNC female connector to be counted by the frequency counter.
21	AM pushbuttons:	
	PULSE pushbutton	When pressed, allows external pulse signals at AM/PULSE connector (19) to amplitude modulate the RF output.
	EXT pushbutton	When pressed, allows external sinusoidal signals at AM/PULSE connector to amplitude modulate the RF output.
	INT pushbutton	When pressed, allows an internal 1 kHz signal to amplitude modulate the RF output.
22	CW pushbutton and indicator	Illuminates when pressed, indicating that unmodulated (CW) operation is selected. Releases all AM and FM pushbuttons.
23	AM LEVEL control	Adjusts the percentage of amplitude modulation of the RF output for internal or external AM operation.

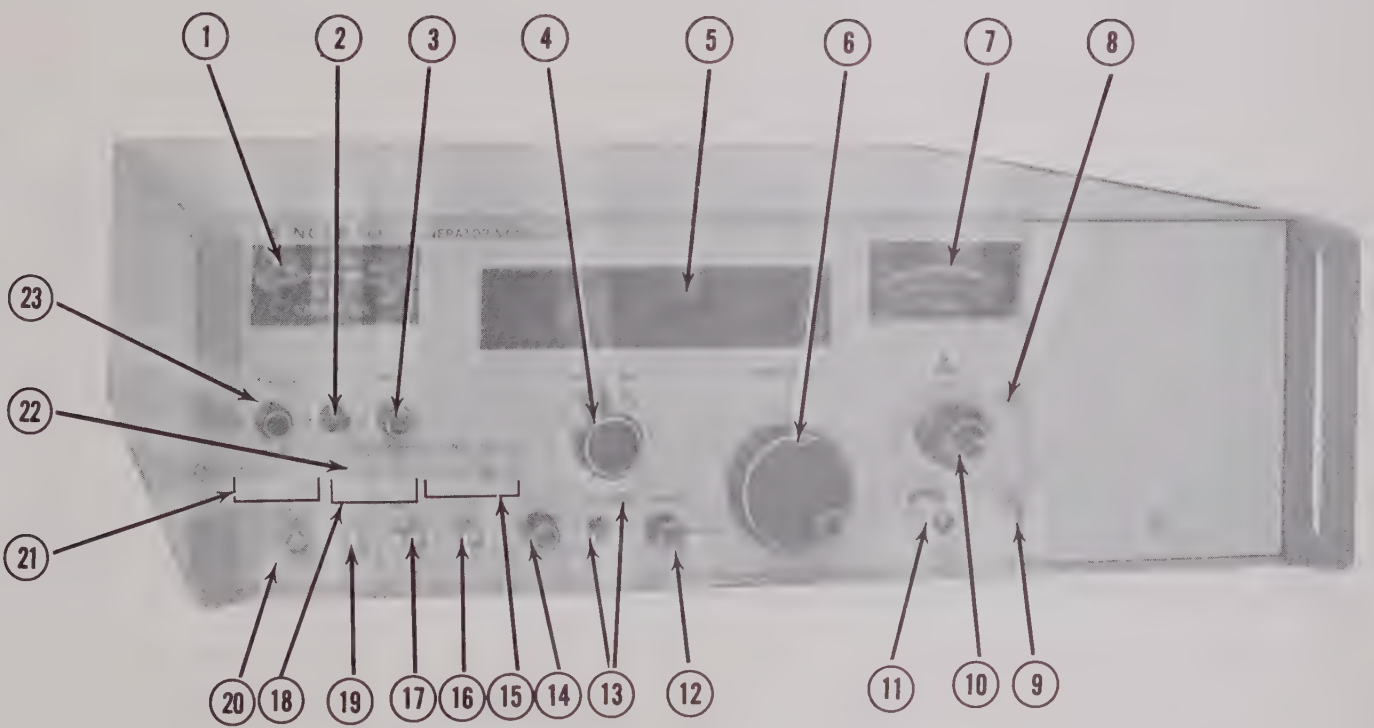


Figure 2-1. Front Panel Operating Controls, Indicators and Connectors

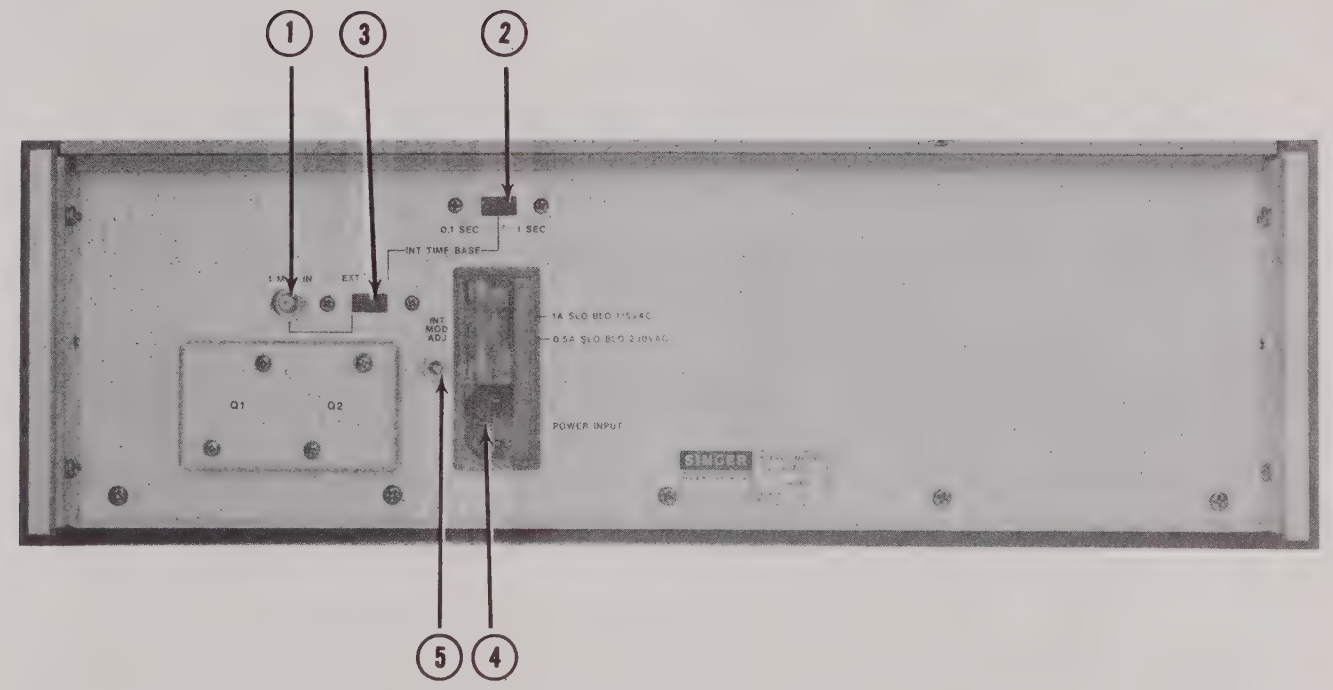


Figure 2-2. Rear-Panel Operating Controls and Connectors

TABLE 2-2. REAR-PANEL OPERATING CONTROLS AND CONNECTORS

Index No. (Figure 2-2)	Control or Connector	Function
1	1 MHz IN connector	BNC connector for coupling an external 1.0 MHz time base signal to the internal frequency counter, when the TIME BASE switch (2) is set to EXT.
2	INT TIME BASE switch	Slide selector switch which provides an internal time base of either 0.1 or 1 second for the external count input.
3	TIME BASE switch	In the INT position, the internal time base is used as a basis for the accuracy of the Signal Generator frequency counter. In the EXT position, an external time base signal of 1.0 MHz may be applied to the 1 MHz IN connector (1), substituting for the internal time base.
4	POWER INPUT assembly:	
	Power receptacle	Polarized three-pin connector through which line power is applied to the Signal Generator.
	115/230 V switch	Slide selector switch which allows the Signal Generator to operate from either 115 VAC or 230 VAC.
5	INT MOD ADJ screwdriver control	Adjusts frequency of internal 1 kHz AM signal to within ±2%.

a. Obtain an unmodulated RF output (refer to paragraph 2-16).

NOTE

For linear amplitude modulation, always maintain the Vx2 pushbutton in the released position during AM operation.

b. Rotate the AM LEVEL control fully counterclockwise, and press the AM EXT pushbutton.

CAUTION

To prevent damage to the Signal Generator, do not apply external modulation signals that exceed a voltage level of 5 volts peak.

c. Couple the external modulation signal to the AM/PULSE connector.

NOTE

External modulation should originate from a source impedance of 600 ohms. A sinusoidal modulating waveform of 2.0 volts rms (nominal) is required for 100% modulation.

d. Set the AM/FM switch to AM.

e. Adjust the AM LEVEL control until the desired percentage of amplitude modulation is indicated on the % AM scale of the % AM/FM DEV meter.

2-22. EXTERNAL PULSE OPERATION.

2-23. To obtain a pulse-modulated RF output using an external pulsed source, proceed as follows:

a. Obtain an unmodulated RF output as described in paragraph 2-17, except do not perform step h at this time.

b. Press the PULSE pushbutton

CAUTION

Do not apply external pulsed signals that exceed a voltage level of 3.5 volts peak.

c. Couple an external pulsed signal to the AM/PULSE connector.

NOTE

In order to produce leveled output pulses as indicated on RF LEVEL meter, the pulsed signal source must be capable of providing in excess of 1.0 volt positive (into 50 ohms). Pulse width must be greater than 4 μsec, with rise and fall times of less than 20 nsec for proper leveling operation.

d. Perform step h of paragraph 2-17.

2-24. INTERNAL FM OPERATION.

2-25. To obtain a frequency-modulated RF output using the internal 1 kHz sine-wave oscillator, proceed as follows:

a. Obtain an unmodulated RF output as described in paragraph 2-17.

b. Rotate the FM DEV control fully counterclockwise and press the FM INT pushbutton.

NOTE

When FM INT pushbutton is pressed, the internal 1 kHz oscillator signal (1.5 volt peak-to-peak) is available at the front-panel 1 kHz MOD OUT connector (source impedance: 1000 ohms).

c. Press the FM CAL push-to-operate control and while holding this control pressed, rotate fully counterclockwise. Upon reaching the fully counterclockwise position, note the last three digits displayed on the frequency digital readout; then, slowly rotate the FM CAL control clockwise until the previously noted digital readout has increased exactly .100 (see example) and carefully release the FM CAL control.

EXAMPLE

Display on digital readout indicates ---.069 (only last three digits are illuminated) with FM CAL control fully ccw. Rotate FM CAL control cw until display has increased in frequency to ---.169.

d. Set the AM/FM switch to FM, and press the FM RANGE kHz pushbutton that corresponds with the peak deviation required.

NOTE

During internal FM operation, the maximum peak deviation obtainable is 0.1% or less of the Signal Generator frequency.

e. Adjust the FM DEV control to obtain the desired FM peak deviation as indicated on the appropriate FM PEAK DEV scale of the % AM/FM DEV meter.

2-26. EXTERNAL FM OPERATION

2-27. To obtain a frequency-modulated RF output, using an external DC to 200 kHz signal, proceed as follows:

a. Obtain an unmodulated RF output as described in paragarph 2-17.

b. Press the FM EXT pushbutton.

c. Press the FM CAL push-to-operate control and while holding this control pressed, rotate fully counterclockwise. Upon reaching the fully counterclockwise position, note the last three digits displayed on the frequency digital readout; then, slowly rotate the FM CAL control clockwise until the previously noted digital readout has increased exactly .100 (see example) and carefully release the FM CAL control.

EXAMPLE

Display on digital readout indicates ---.069 (only last three digits are illuminated) with FM CAL control fully ccw. Rotate FM CAL control cw until display has increased in frequency to ---.169.

d. Set the AM/FM switch to FM, and press the FM RANGE (kHz) pushbutton that corresponds with the peak deviation required.

NOTE

During external FM operation, the maximum peak deviation obtainable is 0.5% of the Signal Generator frequency.

e. Rotate the FM DEV control to the fully clockwise position.

CAUTION

Do not apply external modulation signals that exceed a voltage level of 5 volts peak.

f. Couple an external modulation signal to the FM connector.

NOTE

External modulation should originate from a source impedance of 600 ohms.

g. Adjust the output level of the external modulation source to obtain a full-scale FM PEAK DEV reading. Rotate the FM DEV control to obtain the desired amount of deviation as indicated on the appropriate FM PEAK DEV scale of the % AM/FM PEAK DEV meter.

2-28. CONCURRENT INTERNAL AM/FM OPERATION.

2-29. To obtain an RF output, concurrently amplitude- and frequency-modulated by the internal 1 kHz sine-wave oscillator, proceed as follows:

a. Obtain an unmodulated RF output as described in paragraph 2-17.

b. Perform steps b through d of paragraph 2-19.

c. Perform steps b through e of paragraph 2-25.

2-30. CONCURRENT EXTERNAL AM/FM OPERATION.

2-31. To obtain an RF output, concurrently amplitude- and frequency-modulated by an external modulation source, proceed as follows:

a. Obtain an unmodulated RF output as described in paragraph 2-17.

b. Perform steps b through d of paragraph 2-21.

c. Perform steps b through g of paragraph 2-27.

2-32. CONCURRENT PULSE/FM OPERATION.

2-33. To obtain an RF output, concurrently pulse-and frequency-modulated by external sources, proceed as follows:

a. Obtain an unmodulated RF output as described in paragraph 2-17, except do not perform steps h and i.

b. Perform steps b through d of paragraph 2-23.

c. Perform steps b through g of paragraph 2-27.

2-34. FREQUENCY COUNTER OPERATION.

2-35. The frequency counter digital readout indicates the operating frequency of the Signal Generator. To use the frequency counter to measure external pulse, sinusoidal, or trapezoidal signals from 10 Hz to 10 MHz, proceed as follows:

a. Press the EXT COUNT pushbutton.

b. Set the rear-panel INT TIME BASE switch to the 0.1 SEC position for a frequency resolution of ±10 Hz up to 10 MHz; or to the 1 SEC position for a frequency resolution of ±1 Hz up to 1 MHz. When using the 1 second time base, frequencies up to 10 MHz can be measured to ±1 Hz resolution by dropping off the first digit.

CAUTION

To prevent damage to the Signal Generator, do not apply external signals that exceed a voltage level of 5.0 volts peak.

NOTE

The external signal must have a minimum pulse width (if pulsed signal is used) of 50 nanoseconds, and a minimum amplitude of 200 millivolts.

c. Couple the external signal to the EXT COUNT connector; the digital readout will display the frequency of applied signal in kHz.

NOTE

The maximum frequency that can be read directly by the counter is 9999.99 kHz.

2-36. INTERNAL 1 kHz OSCILLATOR CALIBRATION.

2-37. To adjust the frequency of the internal 1 kHz oscillator, proceed as follows:

a. Connect the 1 kHz MOD OUT connector to the EXT COUNT connector.

b. Press the AM INT and the EXT COUNT pushbuttons. Set AM LEVEL control to mid-range.

c. Adjust rear-panel INT MOD ADJ screwdriver control until the frequency display readout indicates 1000 Hz (±2%).

2-38. INITIAL TESTS.

2-39. The performance standards tests described below may be performed before regular operation of the Signal Generator.

2-40. TEST EQUIPMENT REQUIRED FOR TESTS.

2-41. The test equipment required for the performance standards tests is listed in Table 2-3. Instruments of equivalent characteristics may be substituted for any item listed.

2-42. PERFORMANCE STANDARDS TESTS.

2-43. The performance standards tests delineated in Table 2-4 are a series of tests designed to ascertain whether the Signal Generator is functioning within the specifications of Table 1-1. Should the equipment fail to provide the specified "acceptable indication", the operator should refer to the applicable troubleshooting, repair and/or calibration procedure to correct the defect and return the Signal Generator to proper operating condition. If the unit is within the warranty period, write or telephone the factory before making adjustments other than front and rear panel. Prior to initiating the performance standards tests, couple the Signal Generator to line power as directed in steps a through c of paragraph 2-6. Then set the Signal Generator controls as follows:

Control	Initial Setting
POWER	Pressed
dBm selector switch (outer concentric control)	0/0.3V
dBm vernier level (inner concentric control)	Fully cw
Vx2	Released
VERNIER (attenuation)	Fully cw
FREQUENCY	Any
RANGE MHz	62 - 128
VERNIER (frequency)	Mid-range
CW	Pressed
AM/FM	AM
EXT COUNT	Released
AM LEVEL	Mid-range
INT TIME BASE (rear panel)	0.1 SEC
LOCK/NORMAL	NORMAL

NOTE

Allow the Signal Generator a 30-minute warmup period before performing the steps of Table 2-4. (The major steps of Table 2-4 need not be performed sequentially; however, when performing them out of sequence, the Signal Generator controls should be initially set as indicated above before each major step.)

TABLE 2-3. TEST EQUIPMENT REQUIRED FOR PERFORMANCE STANDARDS TESTS

1. Variac: General Radio W5MT3, 120V 5 amp.
2. Digital Voltmeter: AC/DC Ballantine 355
3. Frequency Counter: HP 5245L
4. Test Oscillator: HP 651A
5. Power Meter: General Microwave Model 454
6. Scope: Tektronix 454A
7. Spectrum Analyzer: SA-70
8. Pulse Generator: Data Pulse Model 101
9. Spectrum Analyzer: SSB-50-1
10. Balanced Mixer: Relcom M1
11. Digital Voltmeter: Cimron 7200
12. FM Discriminator: General Radio 1142A
13. Amplifier: HP 400H
14. Comb Generator: HP 8406A
15. Power Supply: Power Design 4005
16. Attenuator: 10 dB
17. Attenuator: 20 dB
18. Filter: 3 kHz Low Pass Singer
19. Radiometer: Model AFM 2
20. RF Voltmeter: Boonton 91C
21. RF Detector: Singer
22. Kay Electric Attenuators 432C and 432D
23. AC Power Supply, 115V, 47 Hz to 420 Hz, 150W

TABLE 2-4. PERFORMANCE STANDARDS TESTS

1. PRELIMINARY

Paragraphs 2 through 34 give the complete Test Procedure for the 6201 Signal Generator. Each procedure starts with all control settings indicated in paragraph 1.a unless otherwise specified in the individual procedure. During testing, note that each front panel control, with the exception of the pushbuttons, should increase their function with clockwise rotation.

a. Control Settings

CW Switch	Depressed
Output Attenuator	+10 dBm
RF Level Control	Fully CW
V x 2	Depressed
Time Base (Rear Panel)	INT, 1.0 sec.
Range MHz	Band 3
FM Dev. Control	Fully CW
Frequency Vernier	Mid Range
AM Level Control	Fully CW
Ext. Count	Released
Lock/Normal Switch	Normal (Red light out)
Frequency	100 MHz (when energized)

b. Before 6201 is energized ensure mechanical zero of % AM/FM Dev. Meter, M1; and RF Level Meter, M2.

c. Adjust Variac Control for an output voltage of 115V AC ±4V AC. Energize the 6201. Allow the 6201 to stabilize for 30 min. warm-up time before proceeding with this test.

d. Push Button Operation

Verify push button operation in the following manner: The AM Switches, PULSE, EXT and INT are interlocked with each other; FM INT and EXT are also interlocked with each other. These two groups are interlocked with CW switch but are not interlocked with each other. The FM Range switches 30, 100, 300 and 1000, are interlocked with each other but independent of all other groups. All push buttons should be illuminated when depressed, except power.

2. EXT. COUNT OPERATION

Refer to Figure 5 (page 2-22) for Test Setup.

a. Adjust the Test Oscillator to 20 Hz and apply to EXT COUNT input connector. Verify that less than 100 mV rms input signal is required for a correct reading on the 6201 COUNTER. Count on 6201 must be equal ±1 count to count on external counter.

b. Repeat paragraph 2.a with Test Oscillator set for 10,000,000 Hz. Counter accuracy and sensitivity should be the same.

c. Set time base to 0.1 sec and repeat paragraph 2.a. Results should be the same.

d. Repeat paragraph 2.b with time base on 0.1 sec. Results should be the same.

3. FREQUENCY COUNTER OPERATION

Refer to Figure 6 (page 2-22) for Test Setup.

a. Set all controls as specified in paragraph 2.a and adjust 6201 output for 0 dBm.

b. Compare 6201 COUNTER reading with EXT COUNTER reading at the high end and the low end of the 7.75 - 16 MHz range (band 6). Counter readings should match ±2 parts million.

c. Verify that the digits and decimal points at the high and low end of the band are correct.

TABLE 2-4. PERFORMANCE STANDARDS TESTS (CONTINUED)

4. FREQUENCY VERNIER OPERATION

Refer to Figure 6 (page 2-22) for the Test Setup.

a. Adjust 6201 frequency to 16 MHz (band 6) at an output level of 0 dBm.

b. Vary the frequency vernier pot over its entire range. Frequency variation should be greater than 4,800 Hz.

5. 1 kHz OSCILLATOR

Refer to Figure 7A (page 2-23) for the Test Setup.

a. Push AM INT and EXT COUNT buttons. Vary the INT MOD ADJ rear panel control and read the minimum and maximum frequencies. They should be $\leqslant$ 980 and $\geqslant$1020 Hz.

b. Adjust the INT MOD ADJ control to 1 kHz.

c. Connect equipment as shown in Figure 7B (page 2-23) for Test Setup. Measure the amplitude of 1 kHz signal. 1 kHz signal should be free from noise on oscilloscope. Amplitude should be at least 1.5V peak to peak.

d. 1 kHz oscillator should turn off when the AM INT button is released.

6. LINE VOLTAGE VARIATION

Refer to Figure 8 (page 2-23) for Test Setup.

a. Adjust variac for 115 VAC INPUT to 6201 and set all controls as specified in paragraph 1.a. Adjust 6201 for output frequency of 10 MHz.

b. Adjust variac for low (103 VAC), and high (126 VAC), line voltage conditions while observing output power. Power change should not exceed ±0.05 dB.

c. Replace the power meter with a frequency counter and repeat the high and low line voltage variations. Frequency should not change more than ±100 Hz.

d. Set LOCK/NORMAL switch to LOCK MODE and allow 20 seconds to achieve lock. Repeat paragraph 6.b; 6201 should be in LOCK MODE. Frequency should not change more than ±10 Hz. Reset variac to 115 VAC ±4V and reset LOCK/NORMAL to NORMAL MODE.

7. POWER OUTPUT FLATNESS

Refer to Figure 9 (page 2-23) for Test setup. (Note: Do not use pad for this test).

a. Set all controls as specified in paragraph 1.a. Set 6201 for X2 mode and adjust 6201 for +20 dBm output at 100 MHz.

b. Scan each band observing the maximum negative and the maximum positive output power deviations from the reference output. Power variation should not exceed ±0.5 dB for Bands 1 and 2, ±0.25 dBm for Bands 3 through 6.

8. RF LEVEL METER ACCURACY

Refer to Figure 9 (page 2-23) for Test Setup.

a. Set 6201 for X2 mode and adjust the Signal Generator for an output frequency of 100 MHz.

b. Adjust 6201 output power for RF level meter readings of +4 dB, -3 and -10 dB, which should correspond with power output levels of +20, +13 and +6 dBm respectively. Meter readings should be correct ±1.0 dB below 125 MHz, ±1.2 dB above 125 MHz.

c. Set 6201 for X1 mode and 100 MHz. Repeat paragraph 8.b for meter readings of +4 and -3 dB which should correspond to +14 and +7 dBm respectively. Accuracy should be same as in 13.2.

TABLE 2-4. PERFORMANCE STANDARDS TESTS (CONTINUED)

9. PULSE ON/OFF RATIO

Refer to Figure 10 (page 2-24) for the Test Setup.

a. Set the 6201 output power for 0 dBm at X2 mode. (Atten: Attenuator switch at -10 dBm and RF level meter deflection at +4 dB). Push AM PULSE button.

b. Adjust pulse generator for a 1 ms, 4V peak pulse at a PRR of 1000 and connect to the AM/PULSE connector.

c. Adjust CA6A for a full scale reference display of the 6201 output on the log scale with RF attenuator in the 30 dB position.

d. Tune through band 1 through 6 observing the difference is carrier levels (ON/OFF RATIO) on the CA6A. ON/OFF ratio should be $\geqslant$45 dB for Band 1, $\geqslant$60 dB for other bands.

10. MINIMUM PULSE AMPLITUDE

Refer to Figure 10 (page 2-29) for the Test Setup.

a. Set 6201 for 24 MHz and X2 mode.

b. Adjust the pulse generator to MIN level and apply to AM/PULSE connector.

c. Adjust the oscilloscope for a presenration of the RF signal. Push AM/PULSE button. Increase the pulse generator output until the RF output turns ON. The pulse level required to turn the RF power ON should be less than 1V.

11. MINIMUM REPETITION RATE

Refer to Figure 11 (page 2-24) for Test Setup.

a. Set 6201 for 24 MHz and X2 mode and push AM/PULSE button.

b. Adjust the pulse generator for a 50 µsec pulse width at a rep. rate of 10 kHz as displayed on the oscilloscope. Adjust the scope for a full scale presentation.

c. Decrease the pulse generator repetition rate. Pulse amplitude should not decrease more than 10% above 10 Hz repetition rate.

12. MINIMUM PULSE WIDTH

Refer to Figure 11 (page 2-24) for Test Setup.

a. Set 6201 for 24 MHz and X2 mode, and push AM PULSE button.

b. Adjust the Pulse Generator for a repetition rate of 10 kHz and a pulse width of 20 microseconds.

c. Adjust oscilloscope for a 4 cm peak to peak presentation of the pulsed output.

d. Decrease Pulse width until a 10% increase (0.4 cm) in the output amplitude is noted. Pulse width should be less than 4 µsec.

13. PULSE SHAPE

Refer to Figure 11 (page 2-24) for Test Setup.

a. Set 6201 for 24 MHz and X2 mode, and push AM PULSE button.

b. Adjust the pulse Generator for a 5 microsecond Pulse Width.

c. Observe oscilloscope presentation of the pulsed output. Measure the % of over and undershoot. See Figure 12 (page 2-25) for sample measurement. Overshoot and undershoot are not part of the specification, but they should not exceed 35% each.

TABLE 2-4. PERFORMANCE STANDARDS TESTS (CONTINUED)

14. AM METER ACCURACY

Refer to Figure 13 (page 2-25) for Test Setup.

a. Set 6201 for 24 MHz and X1 mode and push AM INT button.

b. Set RF Level Meter for +4 dB meter deflection with X1 mode and measure as follows:

ADJUST AM LEVEL CONTROL FOR THE FOLLOWING SPECTRUM ANALYZER DISPLAY (LIN MODE)		ALLOWED LIMITS OF % AM AS READ ON THE % AM METER
AM Side Band dB Below Carrier	Equivalent AM	
6.0 dB	100%	100% ±8%
10.5 dB	60%	60% ±4.8%
14.0 dB	40%	40% ±3.2%
16.5 dB	30%	30% ±2.4%

c. De-energize AM INT button and push AM EXT button. Connect Test Oscillator to AM/PULSE connector and adjust the Test Oscillator for 20 kHz. Repeat paragraph 14b at 20 kHz AM.

15. EXT. AM FLATNESS

Refer to Figure 14 (page 2-26) for the Test Setup.

a. Set 6201 for 24 MHz and X1 mode and push AM EXT button.

b. Adjust the Test Oscillator and the Oscilloscope for a 30% 1 kHz AM, with full-scale display of the modulation envelope. (Positive half of envelope only.)

c. Tune the Test Oscillator down in frequency. The envelope amplitude should not decrease more than 10% down to DC modulation.

d. Tune the Test Oscillator upward in frequency and find the upper frequency at which a 10% change is noted. This should be >100 kHz.

16. AM DISTORTION

Refer to Figure 15 (page 2-26) for the Test Setup.

a. Set 6201 for 24 MHz and X1 mode. Push AM INT. button. Adjust the AM Level Control for 30% modulation as indicated on the % AM Meter. Adjust RF Level Meter for +2 dB.

b. Set the SSB-50-1 controls as follows:

RF-8	REC-2	CA-5-1
0.0 MHz	Converted 10 Hz - 2 MHz Termination: 600Ω Both 20 dB switches up	Amplitude Scale-Log; Frequency Scale 1.4 kHz/Div.; RF atten. as required.

Adjust the CA-5 RF attenuator switches for a full scale display of the 1 kHz signal. (See Figure 15 (page 2-26) for a sample display.) Measure the largest of second, third or fourth harmonic distortion Pips. It should be at least 34 dB down from the fundamental (1 kHz).

c. Adjust the AM Level control for 70% AM. Repeat paragraphs 16 a and 16 b at 70% AM. Measure the largest of the distortion pips. It should be at least 26 dB down from the fundamental (1 kHz).

TABLE 2-4. PERFORMANCE STANDARDS TESTS (CONTINUED)

17. FM DEVIATION METER ACCURACY

Refer to Figure 3 (page 2-21) for Test Setup.

a. Set all controls as specified in paragraph 1a, adjust 6201 output power to 0 dBm at 30 MHz and push FM EXT. and 30 kHz range buttons.

b. Press FM CAL knob and turn the knob fully CCW, then clockwise until the COUNTER rading increases by 0.100 from the COUNTER reading with knob fully CCW.

Note: When FM CAL. knob is pressed, the first 3 digits from left and kHz/MHz will be blanked off.

c. Apply approximately 12.47 kHz signal from Test Oscillator into FM input connector and set FM DEV. METER for full scale. Vary the frequency of Test Oscillator until the carrier null is observed on CA-6A. The frequency of Test Oscillator at which the carrier null is observed should be between 11.85 and 13.10 kHz.

d. Adjust the Test Oscillator to approximately 8.316 kHz and use FM LEVEL control to set FM DEV. METER for 20 kHz. Vary the frequency of Test Oscillator until the carrier null is observed. The frequency should be tetween 7.693 and 8.940 kHz.

e. Adjust the Test Oscillator to approximately 4.158 kHz and set FM DEV. METER for 10 kHz and vary the frequency of Test Oscillator for the carrier null. The frequency should be between 3.534 and 4.782 kHz.

f. Push 100 kHz range button and tune 6201 to 100 MHz. Repeat paragraph 17b for FM CAL. Repeat paragraph 17c, d, and e ("Carrier Null" procedure) with the following:

FM DEV METER SCALE	TEST OSCILLATOR FREQUENCY	ALLOWABLE RANGE FOR NULL
100 kHz	41.58 kHz	39.50 to 43.66 kHz
60 kHz	24.95 kHz	22.87 to 27.03 kHz
30 kHz	12.47 kHz	10.39 to 14.55 kHz

g. Push 300 kHz Range button and tune 6201 to 300 MHz (band 1). Repeat paragraph 17b for FM CAL. Repeat paragraph 17 c, d and e ("Carrier Null" procedure) with the following:

FM DEV METER SCALE	TEST OSCILLATOR FREQUENCY (STARTING)	ALLOWABLE RANGE FOR NULL
300 kHz	124.7 kHz	118.5 to 131.0 kHz
200 kHz	83.16 kHz	76.93 to 89.40 kHz
100 kHz	41.58 kHz	35.34 to 74.82 kHz

h. Push 1000 kHz Range button and tune 6201 to 500 MHz. Repeat paragraph 17a for FM CAL. Repeat paragraph 17 c, d and e ("Carrier Null" procedure) with the following:

FM DEV METER SCALE	TEST OSCILLATOR FREQUENCY (STARTING)	ALLOWABLE RANGE FOR NULL
1000 kHz	181.1 kHz	172.1 to 190.2 kHz
600 kHz	108.7 kHz	99.63 to 117.7 kHz
300 kHz	54.34 kHz	45.29 to 63.40 kHz

18. FM DISTORTION

Refer to Figure 16 (page 2-27) for the Test Setup.

a. Push FM EXT and 100 kHz Range buttons on 6201. Tune 6201 to 100 MHz. Press the FM CAL. knob and turn knob fully CCW, then clockwise until the COUNTER reading increases by 0.100 from the COUNTER reading with knob fully CCW.

b. Apply 3 kHz signal from Test Oscillator into FM input connector. Set FM DEV METER scale to 100 kHz peak deviation.

TABLE 2-4. PERFORMANCE STANDARDS TESTS (CONTINUED)

c. Tune the Modulation Meter (Radiometer Co. Model AFM2) to 100 MHz test signal. Measure the harmonics of demodulated signal on Spectrum Analyzer SSB-50-1. Largest harmonic should be down at least 40 dB.

Note: Modulation Meter should indicate 100 kHz ±5% peak deviation.

19. INTERNAL FM

a. Tune 6201 to 500 MHz and push FM INT and 1000 kHz Range button. Press FM CAL knob and turn the knob fully CCW, then clockwise until the COUNTER reading increases by 0.100 from the COUNTER reading with knob fully CCW.

b. Turn FM DEV LEVEL control fully clockwise. FM DEVIATION METER should indicate greater than 500 kHz peak deviation. Verify on Data Sheet.

20. RESIDUAL AND INCIDENTAL FM

Refer to Figure 17 (page 2-27) for Test Setup.

a. Set all controls as specified in paragraph 1a.

b. Tune 6201 to 500.10 MHz and adjust the FM Test Setup. The peak deviation in CW mode should not exceed ±125 Hz.

c. Turn LOCK/NORMAL switch to LOCK MODE at 500.10 MHz and allow 20 seconds to achieve LOCK MODE. Adjust the FM setup. The peak deviation in LOCK MODE should not exceed ±125 Hz.

d. Push FM EXT button and tune 6201 to 500.10 MHz. Adjust FM setup. The peak deviation in FM MODE should not exceed ±250 Hz.

e. Repeat paragraph 20b, c and d with the 6201 tuned at 100.10 MHz. The peak deviations in CW, LOCK and FM MODES should not exceed ±25 Hz.

21. INCIDENTAL FM WITH 30% AM

Refer to Figure 18 (page 2-28) for Test Setup.

a. Tune 6201 for 400.10 MHz VX1 mode and push AM INT button. Set AM meter for 30% modulation.

b. Adjust the FM Test Setup. The peak FM deviation should not exceed 300 Hz.

c. Tune the 6201 to 120 MHz and repeat paragraph 21a and 21b. The peak FM Deviation should not exceed 150 Hz.

22. HARMONIC AND SUB-HARMONIC EMANATIONS

Refer to Figure 19 (page 2-28) for the Test Setup

a. Tune 6201 to 512 MHz (Band 1) at an output amplitude sufficient to give a full scale presentation on the analyzer. (Do not exceed -30 dBm input to the Spectrum Analyzer.)

b. Tune the 6201 through its entire frequency range, and observe "worst" case harmonic and sub-harmonic Emanations in each of the six 6201 Frequency Bands. Harmonics should be at least 30 dB down and Sub-harmonics should be at least 45 dB down from fundamental.

Note: Keep analyzer dispersion adjustment for at least 3X the output frequency for second and third order harmonic display.

TABLE 2-4. PERFORMANCE STANDARDS TESTS (CONTINUED)

23. RF LEVEL CONTROL/ATTENUATOR CONTROL

Set all controls as specified in paragraph 1a.

a. Verify that the RF level control and the attenuator control do not bind. Observe the RF level meter reading on the 6201 while switching the attenuator control from the 14 dBm to -130 dBm. The two controls should be mechanically free and independent of each other. The output level of the RF meter should remain constant when switching the step attenuator.

Note: RF output should be terminated with 50 ohm load.

24. RF ATTENUATOR OPERATION

Refer to Figure 19 (page 2-28) for the Test Setup.

a. Set all controls as specified in paragraph 1a. Tune 6201 to 30 MHz at +20 dBm (X2 mode).

b. Adjust CA6A for a fullscale, log presentation of the RF signal.

Note: Be sure not to overload CA6A.

c. Starting at +10 dBm of 6201 output attenuator, reduce the output attenuator in 10 dB steps to -70 dBm of the attenuator. Observe the CA6A presentation. Attenuator response should be accurate ±1.5 dB.

d. Verify proper attenuation from -80 dBm to -140 dBm output by checking the attenuator driver lights visually.

25. LOCK MODE OPERATION

Refer to Figure 6 (page 2-22) for Test Setup.

a. Set all controls as specified in paragraph 1a.

b. Tune 6201 to 500 MHz and set LOCK/NORMAL switch to LOCK MODE. Observe the external counter and measure the time required for the RF output frequency to settle to the frequency reading of 6201 COUNTER. The time should not exceed 20 seconds.

Set LOCK/NORMAL switch to NORMAL MODE and verify that 6201 is in NORMAL MODE. Verify that LOCK light is on in LOCK MODE and off in NORMAL MODE.

c. Repeat paragraph 25b with 6201 tuned at 150 MHz (Band 2), 62 MHz (Band 3), 64 MHz (Band 4), 20 MHz (Band 5) and 7.75 MHz (Band 6). Setting times should not exceed 20 seconds.

d. Tune 6201 to 500 MHz with the FREQUENCY VERNIER at the following three positions; fully clockwise, fully counter clockwise and middle range. Set 6201 to lock mode and verify that 6201 breaks either direction.

e. Repeat paragraph 25d with 6201 tuned at 100 MHz (Band 3), 40 MHz (Band 4) and 7.75 MHz (Band 6).

26. EXT TIME BASE OPERATION

Refer to Figure 20 (page 2-29) for Test Setup.

a. Set all controls as specified in paragraph 1a.

b. Tune 6201 to 100 MHz and apply 1 MHz signal to EXT TIME BASE connector from EXTERNAL STANDARD SIGNAL SOURCE (HP 5245L).

c. Set TIME BASE switch to EXT TIME BASE. Verify that the COUNTER reading of 7201 with EXT TIME BASE is same as that with INTERNAL TIME BASE. Count should be the same ±1.

d. Set TIME BASE switch to INTERNAL TIME BASE.

TABLE 2-4. PERFORMANCE STANDARDS TESTS (CONTINUED)

27. PLUG-IN COMPATABILITY

Refer to Figure 21 (page 2-29) for the Test Setup, with 6202 inserted.

a. Set all controls of 6201 as specified in paragraph 1a and adjust the 6201 Band switch to the Plug-in position.

b. Verify that correct frequency display is on COUNTER at high end of all seven plug-in bands.

c. Set the 6202 to 8.0 MHz. Verify proper operation of the RF output level control with RF Voltmeter. Rotate the RF level control from fully CW to fully CCW at X1 mode and X2 mode. Verify proper RF level output control from +20 dBm to +4 dBm at X2 mode and from +14 dBm to 0 dBm at X1 mode.

d. Verify proper operation of amplitude modulation with spectrum analyzer. Push AM INT button VX1 mode and set AM METER for 30% and 60% mod. by AM LEVEL control. Observe spectrum analyzer and verify the proper display on scope on Data Sheet.

Note: Use Procedure paragraph 14b as reference.

e. Verify proper operation of LOCK/NORMAL MODE with external COUNTER. Repeat paragraph 25b and paragraph 25d with the 6202 tuned at 8 MHz.

f. Verify proper operation of FM DEV meter. Tune 6202 to 8.0 MHz and push FM INT and 300 kHz RANGE buttons. Set FM DEV meter for 1000 kHz peak full scale with FM LEVEL control, then adjust the 6201 band switch to the Band 3 (62-126 MHz) position. The FM DEV meter should indicate 48 kHz ±5 kHz deviation on the 100 kHz peak range. Push CW button and check power level at 8 MHz.

g. Set range switch to Band 3 and select 100 MHz while observing RF LEVEL meter. Power should not change more than ±0.2 dBm from 8 MHz.

28. NOISE OUTPUT

Refer to Figure 22 (page 2-30) for Test Setup.

a. Set all controls of 6201 as specified in paragraph 1a.

b. Set Spectrum Analyzer:

1.	RF ATTENUATOR	0 dB
2.	IF GAIN	
	a. STEP	10 dB
	b. VERNIER	CAL
3.	FREQUENCY DISPERSION	
	a. STEP	130 MHz/Div.
	b. VERNIER	CAL
4.	CENTER FREQ POSITION	400 MHz
5.	BANDWIDTH	
	a. STEP	200 kHz
	b. VERNIER	Fully CW
6.	AMPLITUDE SCALE	LOG
7.	SWEEP TIME	
	a. STEP	30 ms/Div.
	b. VERNIER	CAL
8.	SWEEP/SYNC	INT

29. MASTER OSCILLATOR TUNING RANGE

Set 6201 to Band 1 (248-512 MHz range) and tune Master Oscillator to low end and then to high end. Verify that Master Oscillator reaches stated frequencies.

TABLE 2-4. PERFORMANCE STANDARDS TESTS (CONTINUED)

30. BACKLASH

Refer to Figure 22 (page 2-30) for Test Setup. Tune 6201 to 310 MHz and adjust Spectrum Analyzer for a frequency dispersion of 100 kHz at 310 MHz. Check backlash 20 kHz max.

31. BAND CENTER COMMAND

Tune 6201 to Band 6 (7.75 MHz - 16 MHz Range) and verify proper operation of Band Center Command. Monitor band center voltage at A2A5C1.

Note: Band Center Command output changes state and produces blanking pulse at the following output frequencies.

10.9 MHz ±50 kHz when decreasing frequency. +5V to 0V
11.1 MHz ±20 kHz when increasing frequency. 0V to +5V

32. LOW LEVEL AM DISTORTION

Depress EXT AM Pushbutton, check AM/PULSE BNC center pin to gnd with ohmmeter; with AM level control ccw, resistance should be approximately 1k; at full cw, res. should be 500 ohms.

33. LOW LEVEL FM DISTORTION

Depress EXT FM Pushbutton, check FM BNC center pin to gnd with ohmmeter; with FM DEV control ccw, resistance should be approximately 900 ohms; at full cw, res. should be approximately 700 ohms.

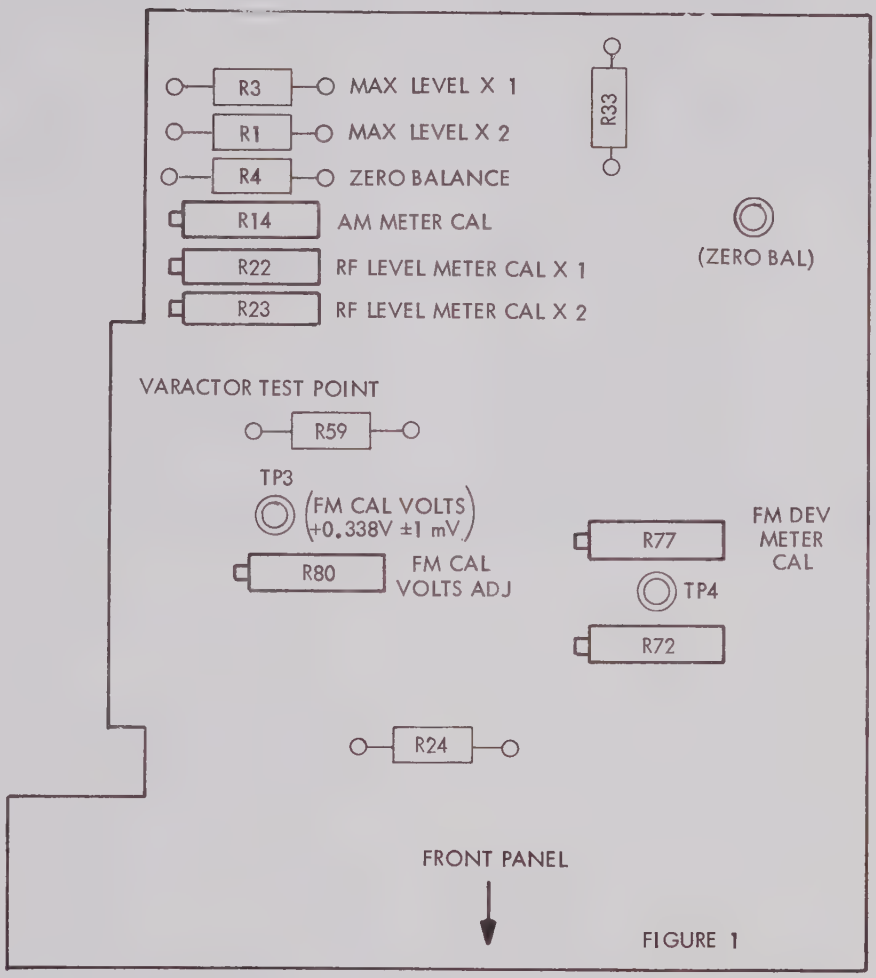


FIGURE 1

TEST SETUP FOR ALIGNMENT OF TRIMPOTS

FIGURE 2

FM DEVIATION METER CAL/ACCURACY

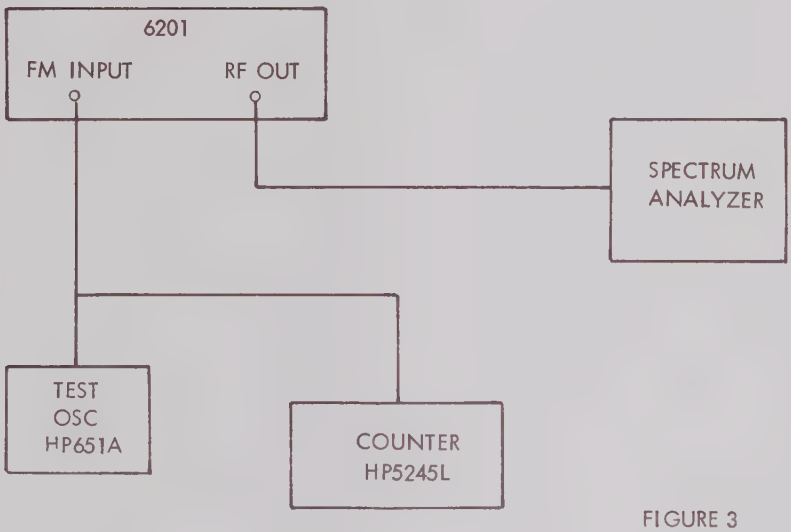


FIGURE 3

TIME BASE CAL

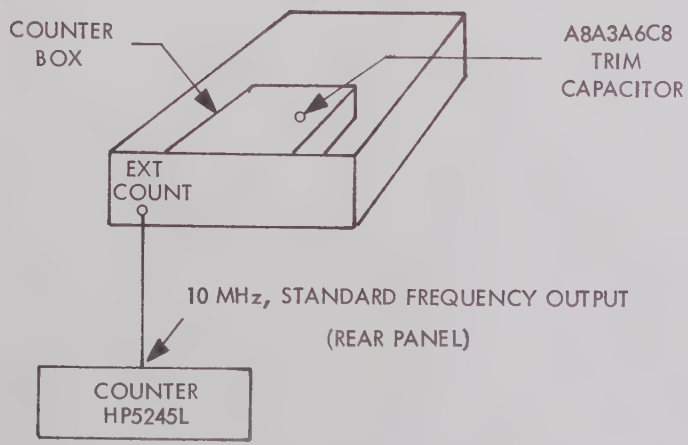


FIGURE 4

EXTERNAL COUNT OPERATION

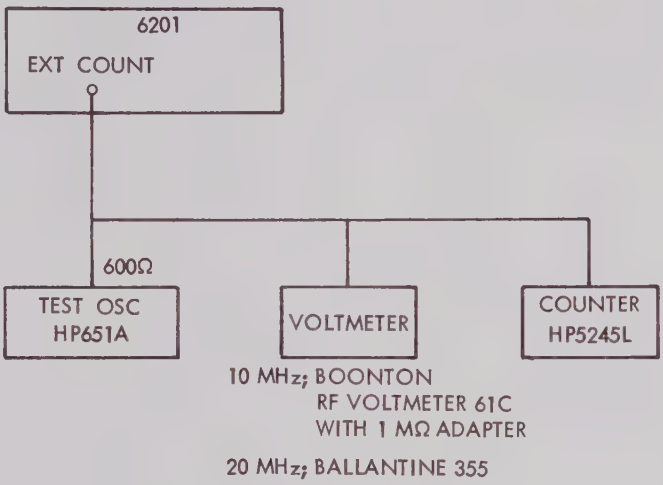


FIGURE 5

FREQUENCY COUNTER/VERNIER OPERATION

FIGURE 6

1 kHz OSCILLATOR OPERATION

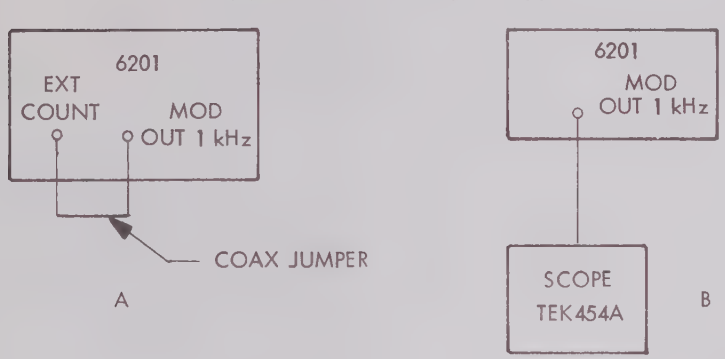


FIGURE 7

LINE VOLTAGE VARIATION

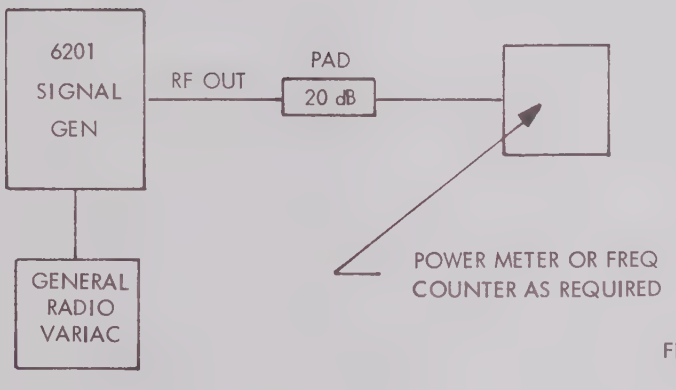


FIGURE 8

POWER OUTPUT

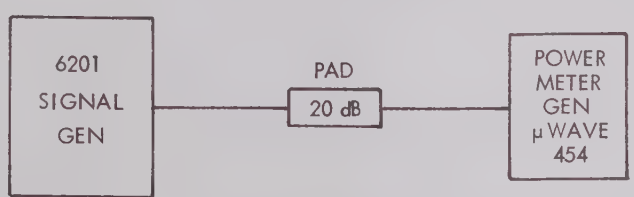


FIGURE 9

PULSE ON/OFF & AMPLITUDE

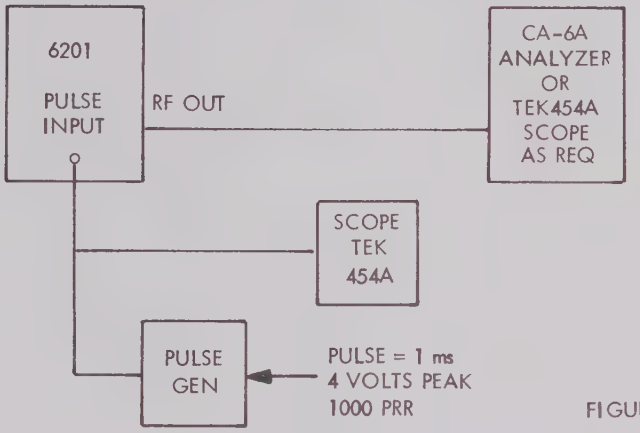


FIGURE 10

PULSE - RATE - WIDTH - SHAPE

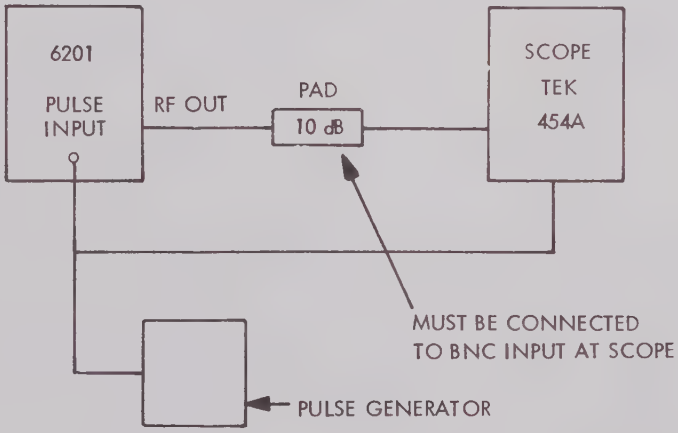


FIGURE 11

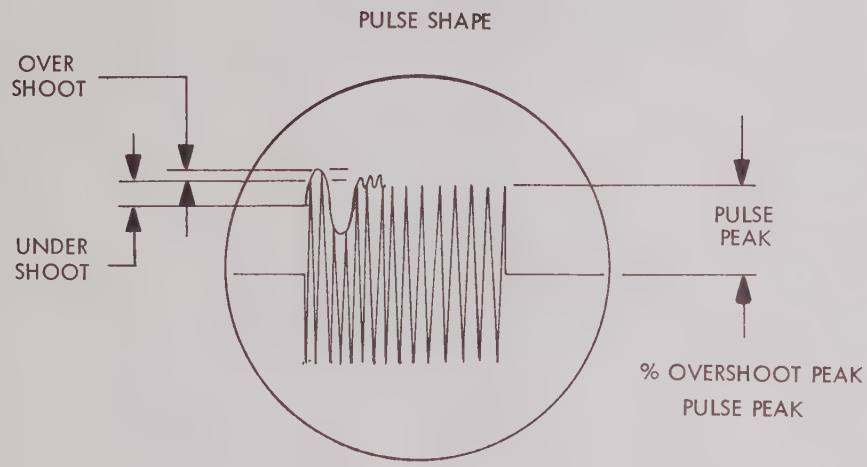


FIGURE 12

AM METER ACCURACY

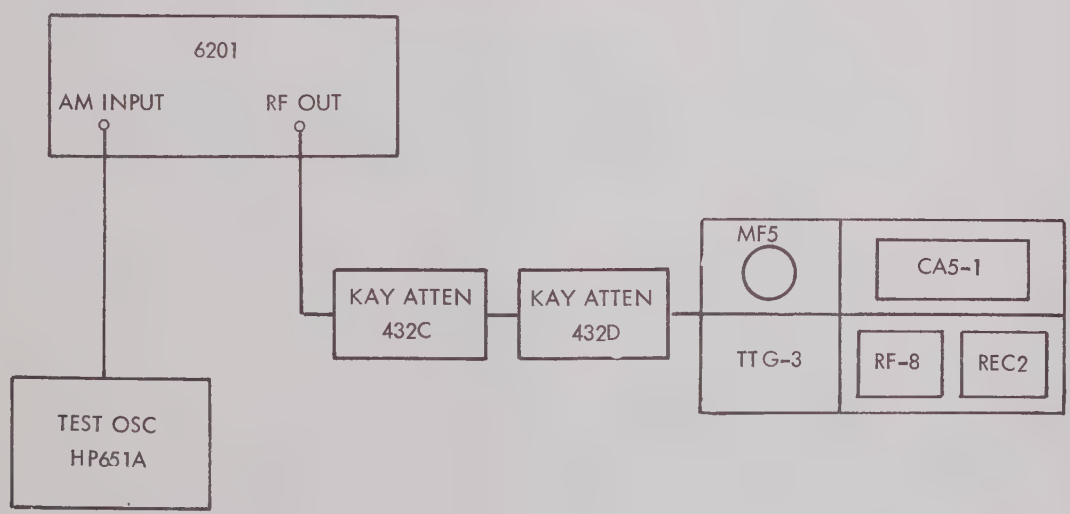


FIGURE 13

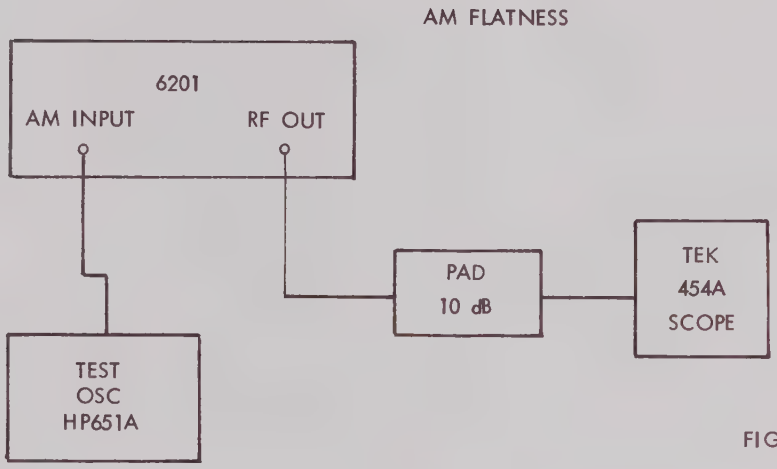


FIGURE 14

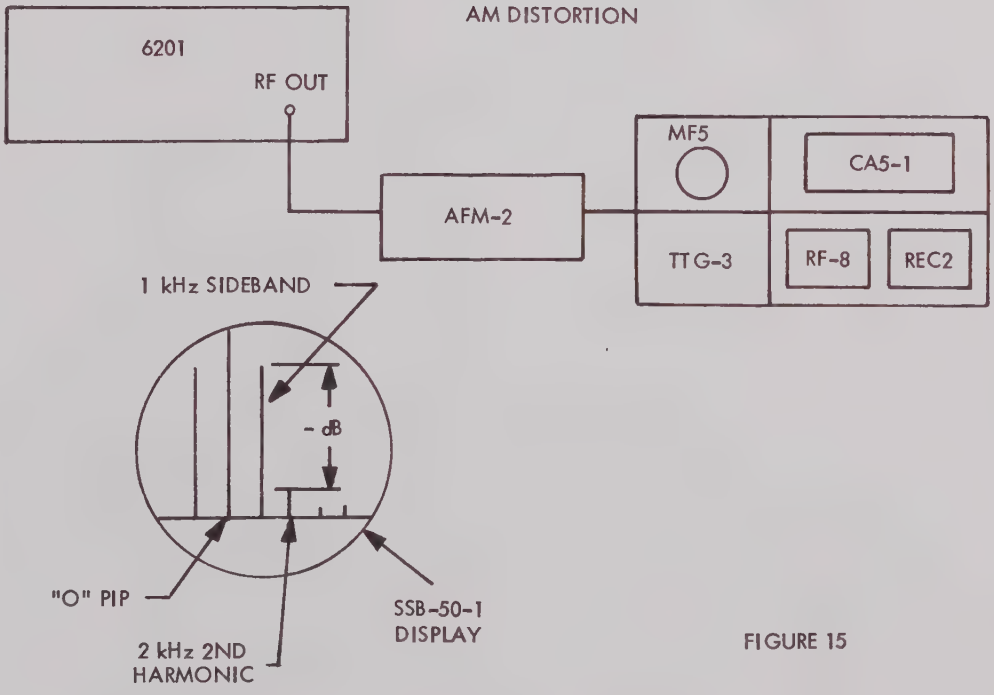


FIGURE 15

FM DISTORTION

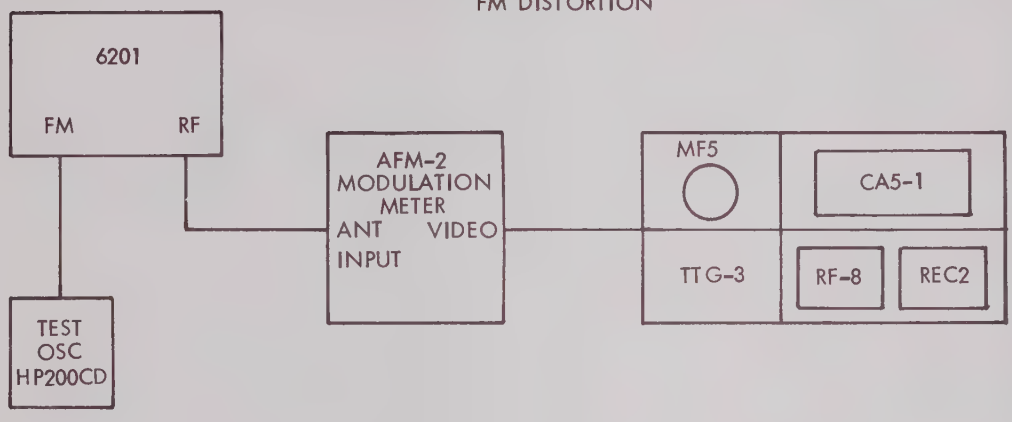
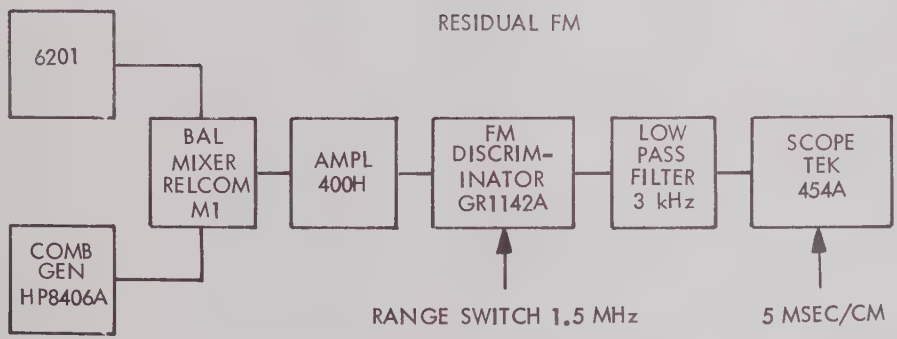


FIGURE 16

RESIDUAL FM

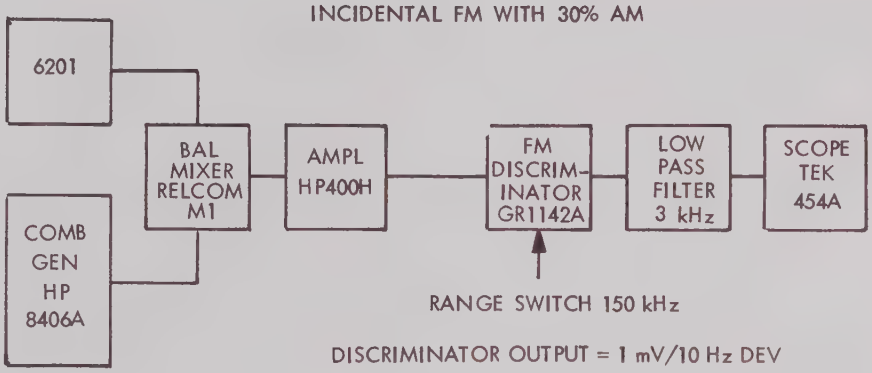


RANGE SWITCH 1.5 MHz 5 MSEC/CM
DISCRIMINATOR OUTPUT = 1 mV/100 Hz DEV

SAME AS B EXCEPT; DISCRIMINATOR RANGE SWITCH SET FOR 150 kHz DISCRIMINATOR OUTPUT = 1mV/10 Hz DEV

FIGURE 17

INCIDENTAL FM WITH 30% AM



DISCRIMINATOR OUTPUT = 1 mV/10 Hz DEV

FIGURE 18

HARMONICS/SUB HARMONICS

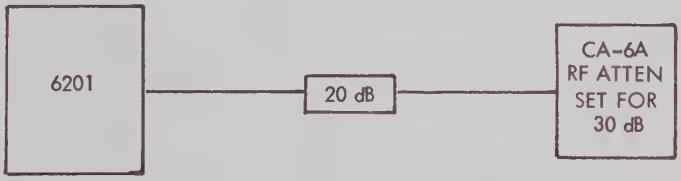


FIGURE 19

EXT TIME BASE OPERATION

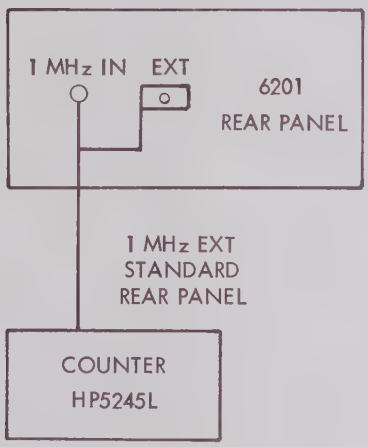


FIGURE 20

PLUG-IN COMPATABILITY

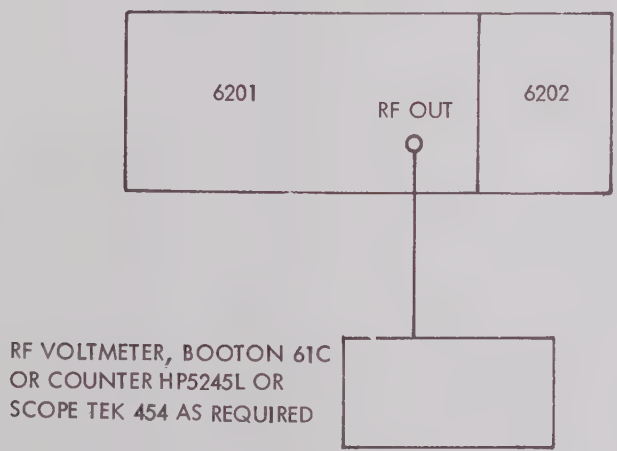


FIGURE 21

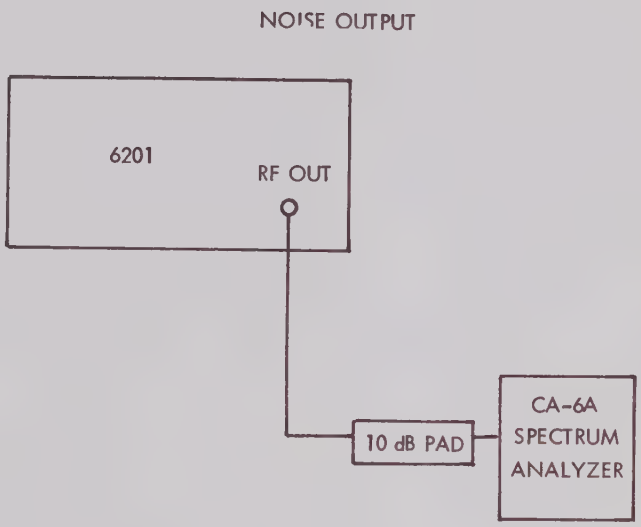


FIGURE 22

SECTION III
THEORY OF OPERATION

3–1. SIMPLIFIED BLOCK DIAGRAM DESCRIPTION.

3-2. The Signal Generator is basically a master/oscillator/power amplifier, with additional frequency divider, modulator, counter/stabilizer, and modulation selection circuits. Figure 3-1 functionally illustrates the Signal Generator in simplified form, ignoring the physical location of its circuits in respect to the assemblies on which the circuits are mounted. Important switches and controls are included to familiarize the user with the function of each.

3-3. The master oscillator is a UHF cavity oscillator that is tunable from 248 to 512 MHz. For all frequency ranges except the highest range (248 - 512 MHz), the oscillator output is divided by a high-speed binary frequency divider, providing six one-octave tuning bands from 7.75 to 512 MHz for the Signal Generator. The master oscillator has applied either a DC to 200 kHz signal for frequency modulation, or a DC voltage for fine frequency tuning.

3-4. The frequency divider output is fed to a balanced modulator for level control (automatic and manual) and amplitude or pulse modulation (when selected) of the RF output. The insertion loss of the balanced modulator can be manually varied over a range of about 16 dB by an adjustable RF level set control in the output of the modulator selection circuit. The modulator output is then coupled to the wideband power amplitude.

3-5. The power amplifier boosts the low level signal from the modulator up to 100 milliwatts maximum (+20 dBm) into 50 ohms. Following the power amplifier, lowpass filters selected by the frequency RANGE MHz control attenuate frequency divider harmonics, and any power amplifier distortion products. A succeeding 150 dB step attenuator operates in conjunction with the adjustable RF level set control to provide a total amplitude range of 166 dB for the Signal Generator output.

3-6. The RF output level is kept flat across the entire frequency range, independent of band switching, by the automatic level control feedback loop. In this feedback loop, the RF output level is detected, and returned to a level control amplifier that continuously compares the output of the detector to a DC reference voltage obtained from the RF level set controls (output of amplitude modulation circuit). The resultant control amplifier output automatically adjusts the insertion loss of the balanced modulator so that the RF level at the detector is kept constant at any level from +4 to +20 dBm. The loop virtually eliminates variations in the RF output level due to changes in master oscillator output level, frequency divider output level, broadband power amplifier gain and other frequency dependent sources of amplitude variation within the loop. The RF detector output is also coupled to the RF LEVEL meter, which indicates the RF output level in conjunction with the attenuator.

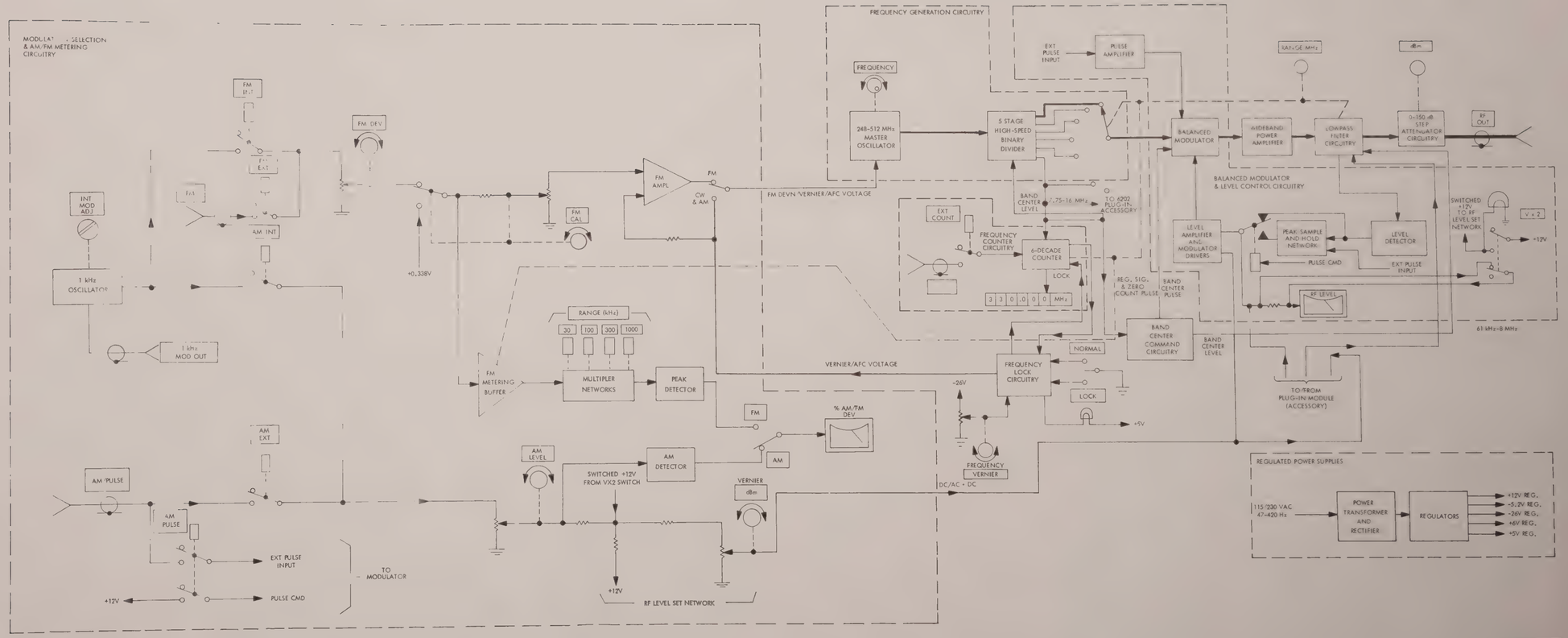
3-7. The modulation capabilities of the Signal Generator include AM, FM and pulse, with negligible interaction when using two modes concurrently (i.e., AM/FM or FM/pulse). When AM operation is selected, the modulation selection and AM/FM metering circuitry injects either an internally-generated 1 kHz signal or an external DC to 100 kHz into the automatic level control feedback loop of the balanced modulator and level control circuitry. The percentage of modulation, which is variable from zero to 100 percent, is indicated on the % AM/FM DEV meter (when selected by the AM/FM switch). When FM operation is selected, either the aforementioned internally generated 1 kHz signal or an external DC to 200 kHz signal is applied to a varactor within the master oscillator cavity structure. Since the FM signal path is direct-coupled, the center frequency, as well as the deviation, can be controlled over a narrow band by the external voltage coupled to the FM connector. The FM peak deviation, which is variable from zero to 1000 kHz, is indicated on the % AM/FM DEV meter (when selected by the AM/FM switch). Pulse modulation is obtained by coupling the external modulating signal at the AM/PULSE connector to the extremely linear and broadband balanced modulator. A sample and hold circuit within the modulator maintains the automatic level control feature operative during pulsed operation.

3-8. The output frequency of the Signal Generator is digitally indicated by a six decade counter which is driven by the lowest output frequency (7.75 - 16 MHz) of the frequency divider. The counter gate interval is automatically programmed by the setting of the RANGE MHz switch to indicate the actual output frequency on six LED (Light Emitting Diode), 7-segment displays. An external signal between 100 Hz and 10 MHz can also be measured by the frequency counter without interrupting normal operation of the Signal Generator.

3-9. The frequency lock circuitry operates in conjunction with the frequency counter. During frequency lock operation, the normal count sequence is interrupted, and the last count is fixed on the LED display. The counter and lock circuits then lock the master oscillator frequency to the frequency indicated on the display. The lock output voltage is fed back to the master oscillator to compensate for frequency drift. In unlocked mode, the VERNIER frequency control output is applied through the lock output circuit for fine frequency tuning. The frequency lock circuit is disabled whenever the counter is used for external count.

3-10. The band center command circuitry generates command level and command pulse outputs from the lowest output frequency of the frequency divider. The band center command level is applied to the frequency divider and low-pass filter circuits to cause filter switching in these circuits to occur near the geometric center (355 MHz) of the master oscillator frequency tuning range; and the band center command pulse is fed to the balanced modulator to blank the Signal Generator output during the band center low-pass filter transition.

3-11. The regulated power supplies convert a 115 or 230 VAC, 47 to 420 Hz power input to five regulated DC outputs (+5, +6, +12, -5.2 and -26 VDC).



3-1

Figure 3-1. 6201 Signal Generator, Simplified Functional Diagram

3–12. DETAILED BLOCK DIAGRAM DESCRIPTION.

3-13. The following paragraphs describe the operation of the functional blocks of the Signal Generator on a detailed block diagram level. For detailed circuit descriptions of the functional blocks, refer to Section IV of this manual.

NOTE

Unless otherwise indicated in any of the logic circuit discussions, a logical ZERO level is 0 volts DC (nominal) and a logical ONE level is +5 volts DC (nominal).

3-14. FREQUENCY GENERATION CIRCUITRY.

3-15. This circuitry consists of the 248 - 512 MHz master oscillator and the frequency divider. The circuitry, which is contained on assemblies A1 and A2, is shown in Figure 3-2 and described in the following subparagraphs.

3-16. 248 - 512 MHz Master Oscillator. The basic 248 to 512 MHz sinusoidal waveform employed to develop all lower signal frequencies is generated by tunable master oscillator A1. The oscillator comprises a UHF power transistor (A1A1Q1) which is coupled to a tunable 1/4 wavelength resonant coaxial cavity. Rotation of the FREQUENCY control mechanically moves a ceramic slug to change the physical length of the cavity, thereby tuning the master oscillator. A varactor diode in the cavity has applied one of the following inputs from the modulation selection and AM/FM metering circuitry (paragraph 3-38): a DC to 200 kHz signal for frequency mdoulation; or a vernier/AFC DC voltage for fine frequency tuning over a range of at least 300 ppm. Output power is extracted by loop coupling at the shorted end of the coaxial cavity.

3-17. Frequency Divider. Two buffer amplifiers (A2A1Q1/Q5 and A2A1Q2) are provided at the input of the frequency divider chain to provide isolation from the master oscillator. The 248 - 512 MHz output of buffer amplifier A2A1Q1/Q5 is applied to the frequency divider chain and the 248 - 512 MHz output of buffer amplifier A2A1Q2 is applied to the RANGE MHz selector. The frequency divider chain is composed of a 5-stage high-speed binary divider. The divider stages are connected in cascade. Each stage has a binary divider (A2A2A1Q1/Q2, A2A2A2Q1/Q2, A2A2A3MC1, A2A3A1MC1, or A2A3A2MC1) and a buffer amplifier (A2A2A1Q3/Q4, A2A2A2Q3/Q4, A2A2A3Q1, A2A3A1Q1 or A2A3A2Q1) for isolation from the succeeding binary divider. The output of each binary divider is applied to a buffer amplifier and to the RANGE MHz selector. The divided output selected by the RANGE MHz selector is applied to the balanced modulator and level control circuitry (paragraph 3-19). The 7.75 - 16 MHz output from divider A2A3A2MC1 is applied (via buffer amplifier A2A3A2Q1) to the frequency counter circuitry (paragraph 3-55) and to the band center command circuitry (paragraph 3-52).

3-18. Two low-pass filters (A2A2A1C1-C3, A2A2A1L1 and A2A2A1CR1; and A2A2A2C1-C3, A2A2A2L1, and A2A2A2CR1) with switchable upper cutoff frequencies are provided in the frequency divider chain. When the output frequency of the master oscillator is below the geometric mean of its range (355 MHz), the band center command input (0 volts) causes the cut off frequency of the filters to be just above the geometric mean of the band. This action causes the filters to attenuate unwanted harmonic products of the divided signals from A2A2A1Q1 and A2A2A2Q1, thereby providing a clean sinusoidal output to drive the modulator. Similarly, when the output frequency of the master oscillator is above the geometric mean, the band center command input (+5 volts) causes the cutoff frequency of the filters to be shifted slightly above the high end of the band, while maintaining a steep skirt. This action again provides a clean output waveform for driving the modulator.

3-19. BALANCED MODULATOR AND LEVEL CONTROL CIRCUITRY.

3-20. This circuitry is principally composed of a wideband preamplifier, two balanced modulators in series, an RF level control circuit, and a sample and hold circuit. The circuitry, which is mostly contained on assembly A3, is shown in Figure 3-3 and described in the following paragraphs.

3-21. Wideband Preamplifier. The 7.75 to 512 MHz signal output from the frequency generation circuitry (paragraph 3-14) is applied to a two-stage wideband preamplifier consisting of RF amplifiers A3A2A1Q1 and A3A2A1Q2. The gain of the preamplifier (which employs degenerative feedback from Q2 to Q1) is approximately 15 dB from 5 to 550 MHz; its output power level is approximately 1 milliwatt (0 dBm).

3-22. Balanced Modulators. The amplified 7.75 to 512 MHz RF output from the wideband preamplifier is applied to first balanced modulator A3A2A2. During the various modes of operation, the insertion loss of this modulator and second balanced modulator A3A2A3 is varied to affect the preamplifier output as follows. In CW, pulsed or FM operation, the DC correction voltage output of the RF level control circuit (paragraph 3-23) varies the RF impedance of the diodes within the balanced modulators to offset any variation in the RF output of the Signal Generator. An AC signal is superimposed on the DC voltage in AM operation, thereby causing amplitude modulation of the preamplifier RF output to be achieved at the balanced modulators. When in pulsed operation, the pulse command (+12 volts DC) from the modulation selection and AM/FM metering circuitry (paragraph 3-38) provides $+V_{cc}$ for inverter A3A1Q1 and initially cuts off the diodes of the balanced modulators, via gates A3A1Q13 and A3A1Q14 and emitter followers A3A1Q12 and A3A1Q15. The external pulse signal from the modulation selection and AM/FM metering circuitry (which is applied through inverter A3A1Q1 and the aforementioned gates and emitter followers to the balanced modulators) then causes the modulator diodes to pass the wideband preamplifier output with minimum loss for the duration of each applied pulse. During band center switching, the balanced modulators are turned off by the blanking pulse from the band center circuitry (paragraph 3-52) in an identical manner as described above for the pulse command.

3-23. RF Level Control Circuit. This circuit consists of RF detector A5A1A1A1 leveling amplifier A3A1MC2, isolation amplifier A3A1Q11, and emitter followers A3A1Q12 and A3A1Q15. A DC reference voltage from the modulation selection and AM/FM metering circuitry (paragraph 3-38) is applied to the inverting input of the leveling amplifier, when in CW, FM or pulsed operation. Also applied to the inverting input of this amplifier (and the RF level meter) is a portion of the RF output at the low-pass filter circuitry (paragraph 3-29), via the RF detector (and the sample and hold circuit when in pulsed

operation). The resulting error (sum) voltage is then amplified and inverted by the leveling amplifier, and coupled through isolation amplifier A3A1Q11 and emitter followers A3A1Q12 and A3A1Q15 to the first and second balanced modulators. Thus, the operating point of the diodes within the balanced modulators is adjusted so that the RF output level remains constant independent of the signal frequency.

3-24. When the Signal Generator is set for AM operation, the leveling amplifier input from the modulation selection and AM/FM metering circuitry consists of the DC reference voltage with superimposed AC. This input results in amplitude modulation of the RF signal at the balanced modulators via the RF level control circuit. During pulsed operation, the +12 volts DC pulse command from the modulation selection and AM/FM metering circuitry gates FET switch A3A1Q10 (via switches A3A1Q7 through Q9). Under this condition, resistor A3A1R35 is bridged across the existing feedback network (A3A1R32 and A3A1C7) of the leveling amplifier, thereby reducing its DC gain.

3-25. The RF LEVEL meter derives its voltage from the summing circuit described in paragraph 3-23. With the VX2 pushbutton in the released position, the meter circuit consists of potentiometer A7R22 in series with RF LEVEL meter M2. Under this condition, the RF LEVEL meter is calibrated to read full scale for +14 dBm at the output of the RF detector. When the VX2 pushbutton is pressed, the following three things occur: +12 volts is switched to the level set network of the modulation selection and AM/FM metering circuitry, thereby increasing the RF output voltage by a factor of 2 and changing the calibration of the RF meter circuit; potentiometer A7R23 is placed is series with A7R22 to compensate for the increased RF output so that meter M2 reads full scale with +20 dBm; and +12 volts is applied to the VX2 indicator, causing it to light.

3-26. Sample and Hold Circuit. This circuit consists of inverters A3A1Q2, A3A1Q4, and A3A1Q5; FET switch A3A1Q6; and unity-gain amplifier A3A1MC1. When in pulsed operation, the external pulse signal coupled to the PULSE/AM connector is applied to inverter A3A1Q2, via the modulation selection and AM/FM metering circuitry (paragraph 3-38). Modulation pulses in excess of +0.5 volts DC drive A3A1Q2 into saturation for the duration of each applied pulse, gating FET switch A3A1Q6 on (via inverters A3A1Q4 and Q5) and allowing capacitor A3A1C11 to charge to the negative output level of RF detector A5A1A1A1. The RF detector output level stored by the capacitor is then coupled through the high input impedance unity-gain amplifier and the normally closed contacts of de-energized relay A3A1K1 to the RF level control circuitry (paragraph 3-23). The R-C time constant of A3A1R20 and A3A1C11 allows the sample and hold circuit to retain the RF detector output during those periods when the modulating pulse is not present, thereby keeping the succeeding RF leveling loop at an operating point comparable to that for CW operation. During pulsed operation, the +12 volts DC pulse command from the modulation selection and AM/FM metering circuitry keeps relay A3A1K1 in the de-energized condition, via switches A3A1Q7 and A3A1Q8.

3-27. WIDEBAND POWER AMPLIFIER.

3-28. The output of the balanced modulator and level control circuitry is coupled to the wideband power amplifier (Figure 3-4), a seven-stage power amplifier chain having a total gain of approximately 50 dB and a 3 dB bandwidth from below 5 MHz to beyond 530 MHz. The output of the power amplifier is applied to the low-pass filter circuitry.

3-29. LOW-PASS FILTER CIRCUITRY.

3-30. The wideband power amplifier output, which is rich in harmonics due to the characteristics of the signal applied, is coupled to the low-pass filter circuitry (Figure 3-4). This circuitry consists of five electronically actuated reed relays (A5A1K1 through K5), a magnetically actuated reed relay (A5A1K6), relay drivers (A5A1A2Q1 through Q3), and a manually-driven filter selector turret switch (A5A4) containing six pairs of low-pass filters. The turret switch is mechanically ganged to the RANGE MHz selector.

3-31. When the RANGE MHz selector is set to any position other than PLUG-IN, the wideband power amplifier output is applied simultaneously to reed relays A5A1K1 and A5A1K3. A band center command voltage, obtained from the band center command circuitry (paragraph 3-53) is applied to switch A5A1A2Q1. When the output frequency of the 248 - 512 MHz master oscillator is below its geometric mean of 355 MHz, the band center command level is 0 volts, causing switches A5A1A2Q1 and A5A1A2Q2 to cut off and switch A5A1A2Q3 to saturate. This, in turn, causes reed relays A5A1K3 and A5A1K4 to energize, thereby inserting the appropriate low end, low-pass filter into the signal path. Each low end filter has an extremely sharp skirt at its high frequency limit to sharply attenuate harmonics of the carrier frequency generated by either the frequency divider, modulator or power amplifier.

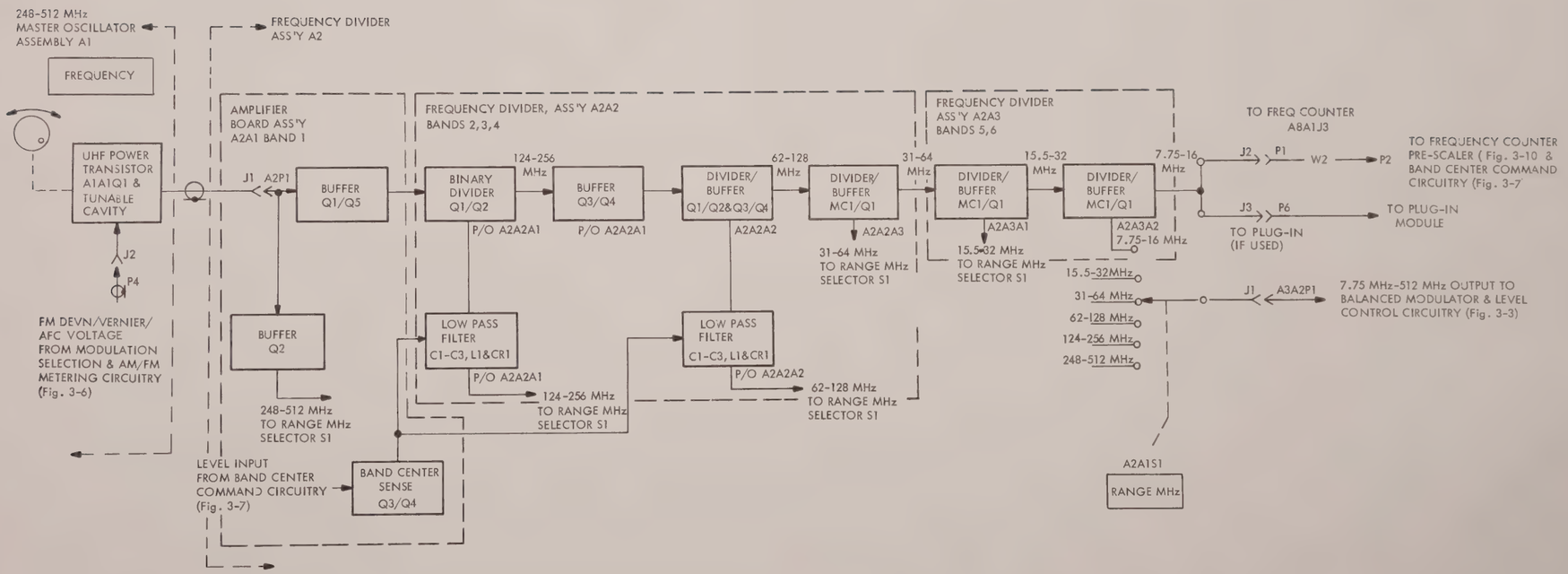
3-32. Similarly, when the output frequency of the master oscillator is above its geometric mean of 355 MHz, the band center command level is +5 volts, causing switches A5A1A2Q1 and A5A1A2Q2 to saturate and switch A5A1A2Q3 to cut off. This, in turn, causes reed relays A5A1K1 and A5A1K2 to energize, thereby inserting the appropriate high end, low-pass filter into the signal path. Each high end filter has an extremely sharp skirt at its high frequency limit to greatly attenuate unwanted harmonics of the carrier frequency.

3-33. The output of the selected low-pass filter (as determined by the setting of the RANGE MHz selector and the operating frequency of the master oscillator) is simultaneously applied to RF level detector A5A1A1A1 and the balanced modulator and level control circuitry (paragraph 3-19); and, through an RC network (A5A1A1R2, A5A1A1C1 and A5A1A1C2) that establishes a 50-ohm output impedance, to the 0 - 150 dB output attenuator circuitry (paragraph 3-35).

3-34. When the RANGE MHz selector is set to the PLUG-IN position, a permanent magnet on the rotor of the turret switch is placed in close proximity to reed relay A5A1K6. Closure of the relay contacts energizes reed relay A5A1K5, thereby allowing the output of the plug-in module (if used) to be coupled to both the RF level detector and the 0 - 150 dB step attenuator circuitry. Resistor A5A1A1R3 establishes the plug-in module output impedance at 50 ohms.

3-35. 0 - 150 dB STEP ATTENUATOR CIRCUITRY.

3-36. The step attenuator circuitry (Figure 3-5) employs two step attenuator assemblies (A6A1 and A6A2) to adjust the RF output level over a 150 dB range, in 10 dB steps.



3-2

Figure 3-2. Frequency Generation Circuitry, Detailed Block Diagram

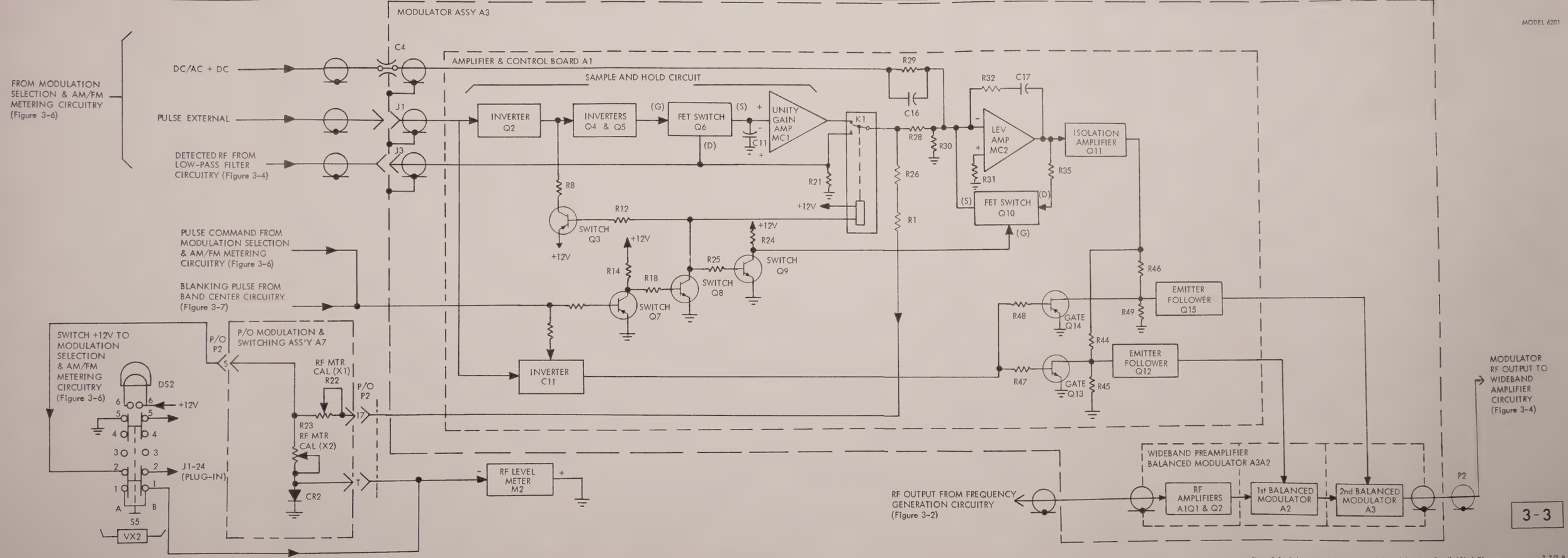


Figure 3-3. Balanced Modulator and Level Control Circuitry, Detailed Block Diagram

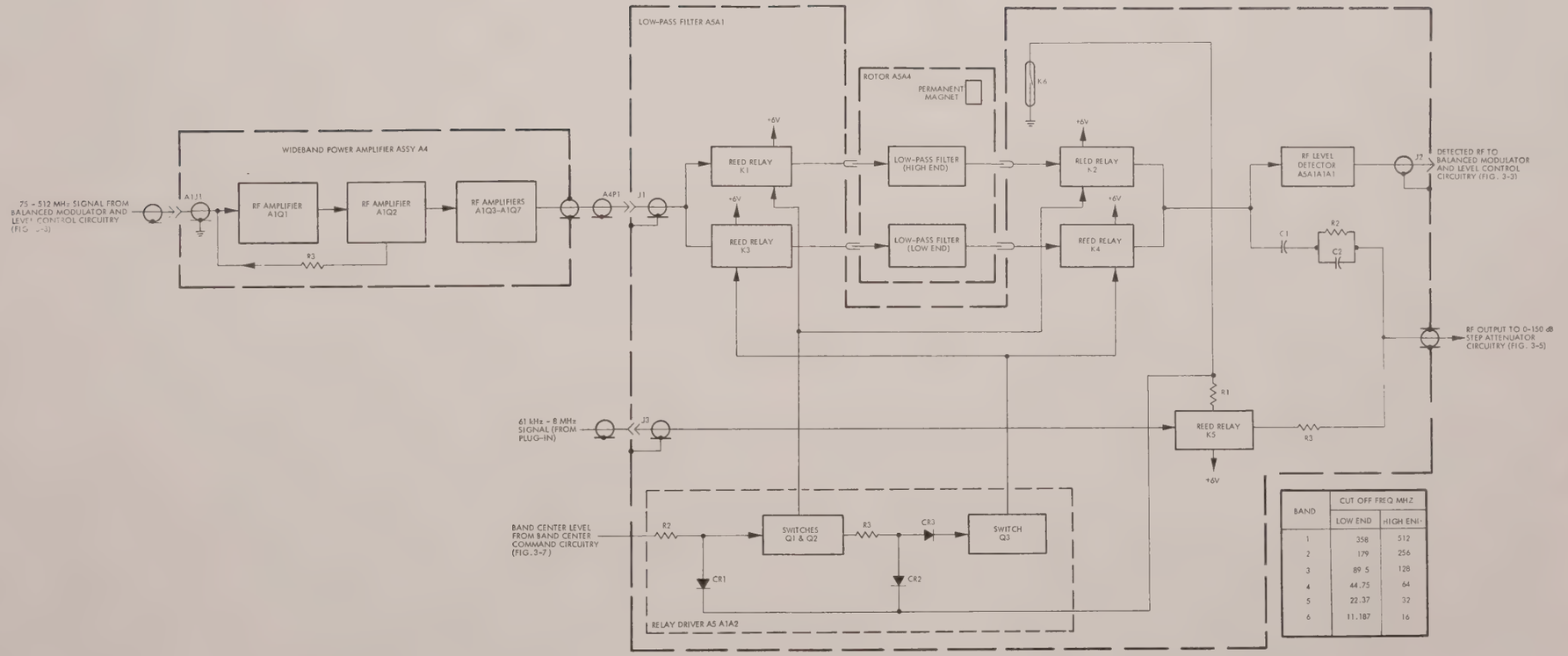


FIGURE 3-4. WIDEBAND POWER AMPLIFIER AND LOW-PASS FILTER CIRCUITRY, DETAILED BLOCK DIAGRAM

3-4

Figure 3-4. Wideband Power Amplifier and Low-Pass Circuitry, Detailed Block Diagram

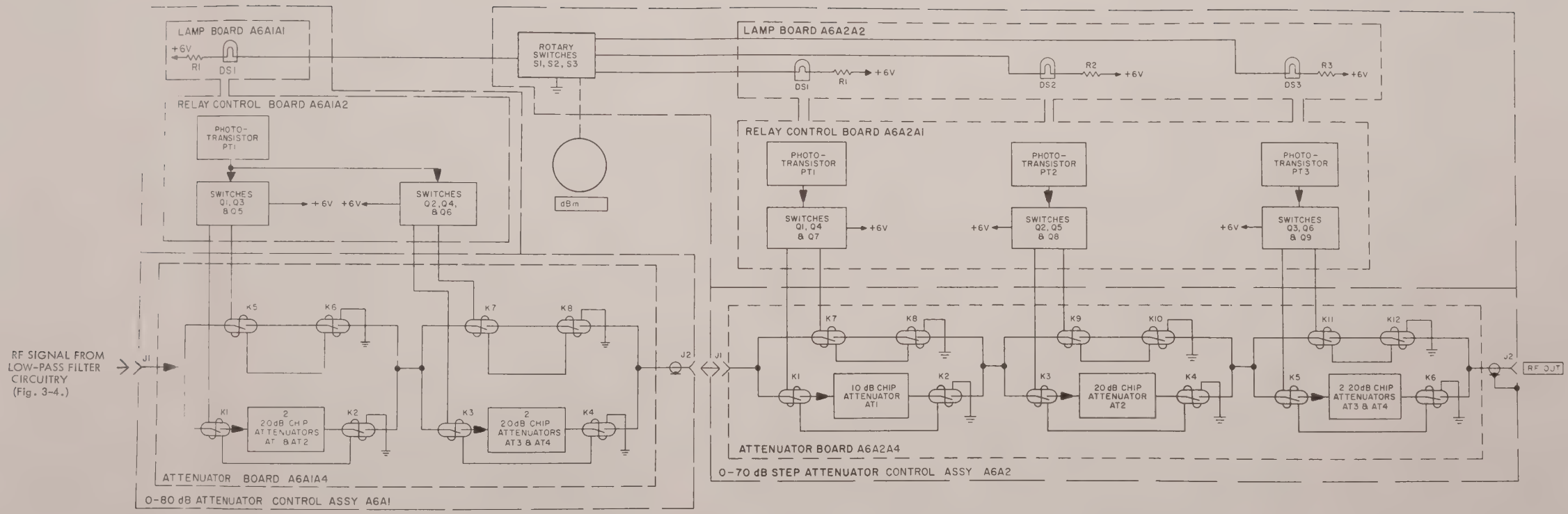


Figure 3-5. 0-150 dB Step Attenuator Circuitry, Detailed Block Diagram

One attenuator assembly (A6A2) consists of 10 dB, 20 dB, and 40 dB chip (two 20 dB chips in series) attenuators, which provides up to 70 dB of attenuation in 10 dB steps. The other attenuator assembly (A6A1) contains four 20 dB, a total of 80 dB which is inserted in one step. The desired attenuation, from 0 to 150 dB, is obtained by inserting and bypassing various combinations of the 10, 20, 40 and 80 dB attenuators as indicated in Table 3-1 and described below.

3-37. When the dBm switch is set to +10/1.0V, all attenuators are bypassed. Lamps A6A1A1DS1 and A6A2A2DS1 through DS3 are out since the path to ground through the dBm switch wafers is not completed. Under this condition, examine the state of the 10 dB chip attenuator. Since lamp A6A2A2DS1 is not illuminated, phototransistor A6A2A1PT1 is in cutoff, placing both A6A2A1Q1 and A6A2A1Q4 in saturation and A6A2A1Q7 in cutoff. Saturation of A6A2A1Q4 energizes the coils which activate reed relays A6A2A4K7 and A6A2A4K8 to bypass the 10 dB chip attenuator, while A6A2A1Q7 in cutoff opens reed relays A6A2A4K1 and A6A2A4K2 to open circuit the chip. The same occurs when the dBm switch is set to any odd decade value (e.g., -10, -30, -50, etc.). The opposite results when the dBm switch is set to even decade values (e.g., 0, -20, -40, etc.). Lamp A6A2A2DS1 illuminates, phototransistor A6A2A1PT1 conducts, placing both A6A2A1Q1 and A6A2A1Q4 in cutoff and A6A2A1Q7 in saturation. The 10 dB chip attenuator is then inserted into the RF signal path. The same sequence of events occurs for the 20 dB and 40 dB steps of attenuation. The 80 dB step attenuator is also similar in operation, except that all four 20 dB chips are connected in series by reed relays A6A1A4K1 through K4 or all four are bypassed by reed relays A6A1A4K5 through K8. The reed relays are actuated by parallel switching circuits A6A1A4Q1 through A6. The attenuator output is available at the front panel RF OUT jack.

TABLE 3-1. dBm SWITCH SETTING VS STEP ATTENUATOR INSERTION

dBm Switch Setting	Attenuation Inserted			
	10 dB Chip	20 dB Chip	40 dB Chip	80 dB Chip
+10/1.0V				
0/0.3V	X			
-10/.10V		X		
-20/.03V	X	X		
-30/10 mV			X	
-40/3 mV	X		X	
-50/1.0 mV		X	X	
-60/0.3 mV	X	X	X	
-70/.10 mV				X
-80/.03 mV	X			X
-90/10 μV		X		X
-100/3 μV	X	X		X
-110/1.0 μV			X	X
-120/0.3 μV	X		X	X
-130/.10 μV		X	X	X
-140/.03 μV	X	X	X	X

3-38. MODULATION SELECTION AND AM/FM METERING CIRCUITRY.

3-39. The modulation selection and AM/FM metering circuitry is mostly contained on assembly A7. The circuitry is shown in Figure 3-6 and described in the following sub-paragraphs.

3-40. CW Operation. When the front-panel CW push-button (A7S4) is pressed, all modulation pushbuttons are released. Under this condition, the internal 1 kHz oscillator (paragraph 3-51) is de-energized and all external modulation signals coupled to the Signal Generator are disconnected by AM PULSE pushbutton A7S1, AM EXT pushbutton A7S2 and FM EXT pushbutton A7S5. In addition, with the AM PULSE pushbutton released, the generation of a pulse command (paragraph 3-42) is inhibited.

3-41. The regulated +12 volts supply output is applied to the RF level set network consisting of resistors A7R3 and A7R1, and dBm vernier control A6A1R1 in parallel with A7R5; this produces a DC reference voltage of approximately +4 volts across A6A1R1 with front-panel VX2 pushbutton S5 in the released position. When the VX2 pusybutton is pressed, switched +12 volts is applied to the junction of A7R3 and A7R1 (effectively bypassing A7R3 in the level set network), thereby increasing the DC reference voltage to approximately +8 volts. The resulting DC reference voltage output from the dBm vernier control varies the insertion loss of the balanced modulators of the balanced modulator and level control circuitry (paragraph 3-19) over a dynamic range of typically 60 dB. When in CW operation, +12 volts is applied to CW indicator A7DS1 (via the released modulation selector push-buttons), causing it to illuminate.

3-42. Pulsed Operation. When AM PULSE pushbutton A7S1 is pressed (thereby releasing the AM INT and AM EXT push-buttons), a pulse command (+12 volts) and the external pulse input at AM/PULSE connector J10 are applied to the balanced modulator and level control circuitry (paragraph 3-19). In pulsed operation, the RF level set network operates identically as when in CW operation (paragraph 3-40).

3-43. Amplitude Modulation. When AM EXT pushbutton A7S2 is pressed (thereby releasing the AM PULSE and AM INT pushbuttons), the Signal Generator is set for external AM operation. In this mode of operation, the external AM signal coupled to AM/PULSE connector J10 is applied through AM LEVEL control R1 to both the RF level set network (A7R1, A7R3, A7R5 and A6A1R1) and AM metering buffer amplifier A7Q1. At the level set network, the AM signal is superimposed on the DC reference level; the resulting AM + DC signal is then applied to the balanced modulator and level control circuitry (paragraph 3-19) where actual amplitude modulation is achieved. Note that when in AM operation, the VX2 pushbutton must be in the released position. This limits the maximum unmodulated RF output power level during AM operation to +14 dBm, thereby permitting modulations of up to 100% to be attained at full rated output power (+20 dBm).

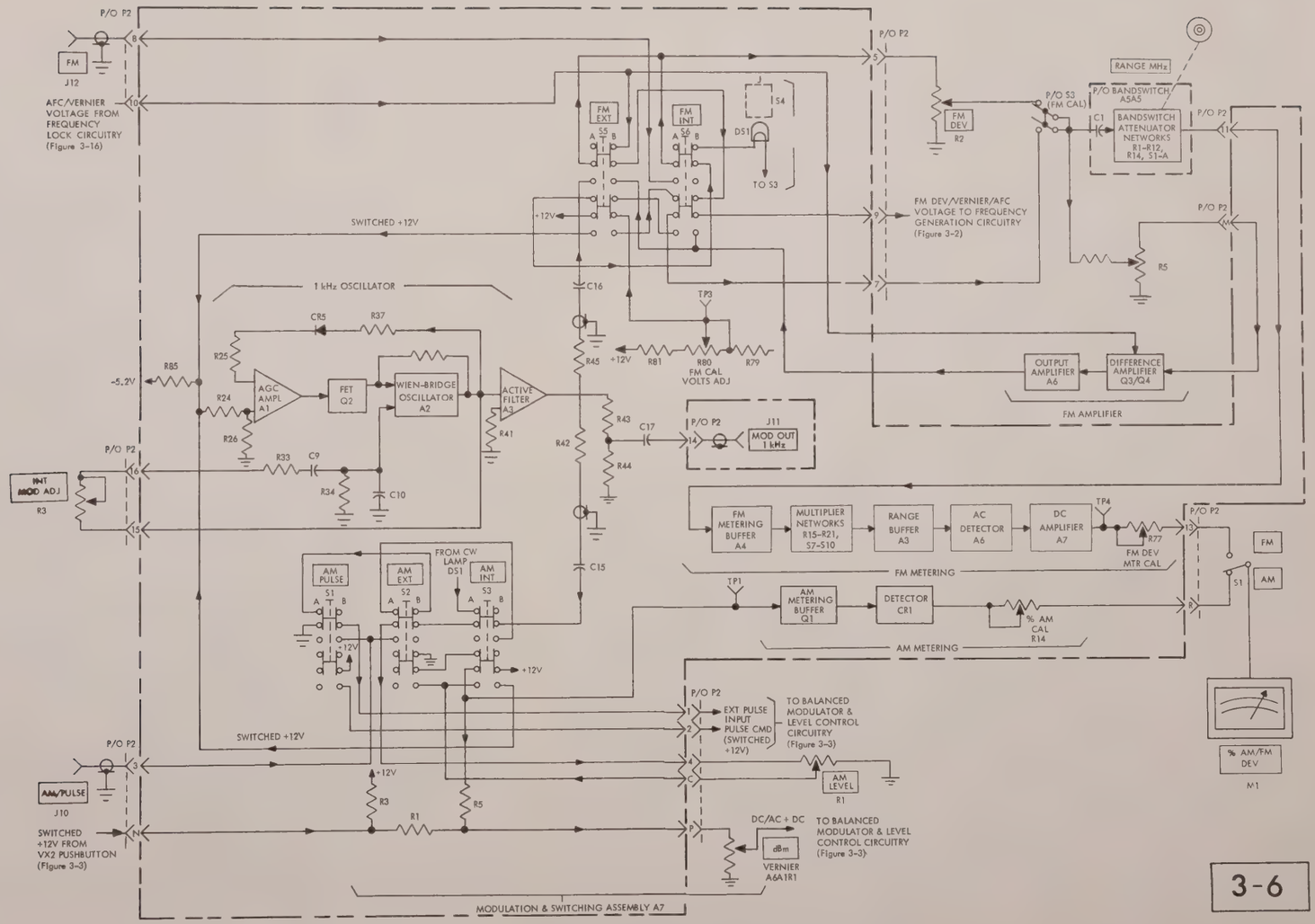
3-44. The external AM signal at the output of AM metering buffer amplifier A7Q1 is detected by A7CR1 and the resulting DC signal (which is proportional to the modulating signal level) is routed through % AM calibration screwdriver control A7R14 to AM/FM selector switch S1. When this switch is set to AM, the DC signal is applied to % AM/FM DEV meter M1, where a visual indication of the percentage modulation is presented. Note that, since the modulating signal level is superimposed on the DC reference level, adjustment of dBm vernier control A6A1R1 has no effect on the percentage modulation for a given setting of the AM LEVEL control.

3-45. When AM INT pushbutton A7S3 is pressed (thereby releasing the AM PULSE and AM EXT pushbuttons), the internal 1 kHz oscillator (paragraph 3-51) is energized. The 1 kHz tone is then applied through the AM LEVEL control to the RF level set network and the AM metering buffer amplifier. At this time, any external modulation signal coupled to the AM/PULSE connector is open-circuited.

3-46. Frequency Modulation. When FM EXT pushbutton A7S6 is pressed (thereby releasing the FM INT pushbutton), the Signal Generator is set for external FM operation. The external FM signal at FM connector J12 is coupled through FM DEV R2 and closed contacts 1 and 2 of released FM CAL switch S3 to both stage A7Q3A of an FM amplifier (via FM CAL control R5) and FM metering buffer amplifier A7A4 (via one of six bandswitch attenuator networks). After amplification by A7Q3/Q4 and A7Q6, the external FM signal is applied to the varactor within master oscillator A1. FM DEV control R2 permits adjustment of the frequency deviation obtained by a given modulating signal, while VERNIER frequency control R4 permits fine tuning of the master by adjusting the quiescent DC operating point of A7Q3B, via the frequency lock circuitry (paragraph 3-79). When the FM EXT and FM INT pushbuttons are both released, the external FM signal is disconnected from the master oscillator varactor. Under this condition, only the vernier tuning signal is applied to the master oscillator.

3-47. The six bandswitch attenuator networks at the input of FM metering buffer amplifier A7A4 ensure that the peak deviation indicated on the % AM/FM DEV meter corresponds with the actual deviation of the RF output frequency. In band 1, the FM deviation sensitivity is 0.338 volt/100 kHz peak deviation. The deviation sensitivity decreases by 50% for each successive band (e.g., 0.338 volt/50 kHz peak deviation for band 2, 0.338 volt/25 kHz peak deviation for band 3, etc.). The external FM signal at the output of FM metering buffer amplifier A7A4 is routed through range buffer amplifier A7A5 (via one of four meter multiplier networks), AC detector A7A6, and DC amplifier A7A7 to AM/FM selector switch S1. When this switch is set to FM, the DC output of A7A7 is applied to % AM/FM DEV meter M1, where a visual indication of the deviation sensitivity is presented. Precision resistors A7R15 through R21, in conjunction with FM RANGE (kHz) pushbuttons A7S7 through S10, function as FM meter multipliers.

3-48. Calibration of the deviation sensitivity is accomplished by means of an internal +0.338 volt reference obtained from the +12 volt power supply through the voltage divider consisting of precision resistors A7R79 through R81. When FM CAL pushbutton S3 is pressed, the +0.338 volt reference level is coupled to the FM amplifier in place of the external modulating signal. The desired deviation sensitivity is obtained by initially adjusting FM CAL control R5 from the maximum counterclockwise position until exactly an increase of .100 is observed on the frequency counter display. The FM CAL switch is then placed in the released position and



3-6

Figure 3-6. Amplitude Modulation, AM Metering and Demodulators Circuitry, Detailed Block Diagram

the FM DEV control is adjusted until the desired sensitivity is observed on the % AM/FM DEV meter.

3-49. As in the case for AM operation, the Signal Generator can be frequency modulated by the internal 1 kHz oscillator (paragraph 3-51). When FM INT pushbutton A7S5 is pressed (thereby releasing the FM EXT pushbutton), the 1 kHz oscillator is energized. The 1 kHz tone is then coupled to the FM DEV control in place of the modulating signal applied to the FM connector.

3-50. Concurrent Modulation. Paragraphs 3-40 through 3-49 detail the operation of each modulation mode. By simply set ing the Signal Generator for simultaneous operation in two independent modes (one being frequency modulation and the other being either amplitude or pulse modulation), concurrent AM/FM or FM/pulse outputs can be obtained.

3-51. Internal 1 kHz Oscillator. A 1 kHz audio signal for internal amplitude modulation or frequency modulation of the RF output is generated by Wien bridge oscillator A7A2, when AM INT pushbutton A7S3 or FM INT pushbutton A7S5 is pressed. When either of these pushbuttons is pressed, +12 volts is applied to AGC amplifier A7A1, causing FET A7Q2 to be gated on. This, in turn, causes the Wien bridge oscillator to be energized. The oscillator output, which may be varied ±2 percent of 1 kHz by rear-panel INT MOD ADJ screwdriver control R3, is coupled through active filter A7A3 (which eliminates any distortion in the oscillator output) to 1 kHz MOD OUTPUT connector J11 and to the AM and/or FM circuits. Any variation in the oscillator output level is sensed by detector A7CR5, amplified by A7A1, and applied to the FET, which acts as a variable resistor to maintain the output level constant.

3-52. BAND CENTER COMMAND CIRCUITRY.

3-53. The 7.75 to 16 MHz output from the final stage of the frequency divider chain (paragraph 3-17) is used by the band center command circuitry (Figure 3-7) to generate the band center command level and pulse signals. The input circuit consists of an amplifier/limiter (A8A3A6Q6, Q5). The output of the amplifier/limiter circuit is coupled to a low-pass filter whose insertion loss is approximately 5 dB at 11.093 MHz. This frequency corresponds to the geometric mean (355 MHz) of the master oscillator tuning range. The low-pass filter output is applied to detector A8A3A6CR1, which is used to drive Schmitt trigger A8A3A6Q1/Q2. Since the detector polarity is negative, the input to the base of A8A3A6Q1 goes positive as frequency increases. The result is that, at the high end of the frequency band, A8A3A6Q1 is saturated and A8A3A6Q2 is cutoff. Potentiometer A8A3A6R1 adjusts the Schmitt trigger hysteresis so that the trigger switches at about 11.1 MHz when tuning up in frequency, and at about 10.9 MHz when tuning down. Potentiometer A8A3A6R2 adjusts the DC bias level on which the detector output rides.

3-54. The output of the Schmitt trigger is fed to two gate circuits (A8A3A6Q3 and Q4), and then to a delay logic circuit (A8A3A6IC1/IC2). The delay logic circuit has two outputs: the first output is the band center command level, which is logical ZERO at the low end of the frequency band, and logical ONE at the high end of the frequency band. The other delay logic output is a positive-going pulse that drives an output monostable multivibrator (A8A3A6IC3). The quiescent output state of the delay logic is logical ZERO; at band center transitions, the output is a positive pulse. The delay logic output pulse then drives the output monostable multivibrator circuit, which generates the band center blanking pulse.

3-55. FREQUENCY COUNTER CIRCUITRY.

3-56. This circuitry, which is contained on assembly A8, performs the following functions: it provides a highly accurate frequency measurement of the Signal Generator output signal or an external signal from 100 Hz to 10 MHz; and it operates in conjunction with the frequency lock circuitry (paragraph 3-79) to give crystal stability of the Signal Generator output signal. The following subparagraphs provide a description of the overall operation of the frequency counter circuitry, and a detailed block diagram description of each of its functional circuits.

3-57. Counter Overall Operation. In the normal count mode (unlock operation), the counter circuitry counts the number of pulses (f_c) that are gated during a selected count interval (ΔT). The count (product of f_c and ΔT) is then stored and displayed directly on a six-digit LED readout, together with the range. During external count operation, a fixed count interval is employed to directly count the applied signal frequency.

3-58. In the frequency lock mode, the count operation is inverted. The counter counts the f_c pulses backward to zero. At the zero count, the counter generates a LOAD command which pre-sets the counter with the stored number and a ZERO pulse that drives the frequency lock circuitry. This circuitry, in turn, compares the timing of the ZERO pulse with the timing of a stable reference signal from the frequency counter circuitry. The resulting DC signal from this comparison is then used to control the frequency of the master oscillator.

3-59. Figure 3-8 is a block diagram of the frequency counter. The 7.75 to 16 MHz output from the frequency divider chain (paragraph 3-17) is used to generate the f_c pulses. The count input is divided by the pre-scaler circuitry, which has five division ratios: 2 (for frequency lock), 8, 16, 32 and 64. The correct sub-harmonic is selected by the f_c gate commands from the control logic circuitry, which is controlled by the frequency RANGE MHz selector and the band logic circuitry. The f_c pulse output from the pre-scaler is applied to the counter/storage circuitry.

3-60. In the normal count mode, the duration of the count is controlled by the UPGATE command from the time base generator circuitry. The counter/storage circuitry counts the f_c pulses for the duration of the UPGATE command (ΔT) period, and then stores that number upon command from the time base generator circuitry. The storage has six four-bit BCD display outputs that drive the display. The count being stored is displayed by the six digit display assembly. After the count is stored, the time base generator circuitry clears the counter in preparation for the next cycle. Figure 3-9 shows the normal count mode timing sequence.

3-62. The time base generator circuitry controls the timing functions of the frequency counter and the frequency lock circuitry. Timing is derived from either a 4 MHz oscillator whose output is divided by four to obtain a stable 1 MHz signal; or an external stable 1 MHz signal. The selected

1 MHz signal is further divided to determine the UPGATE command period, and the timing of the STORE and CLEAR commands. As in the case of the pre-scaler circuitry, the division ratio is determined by the band logic circuitry (via the control logic circuitry) as a function of frequency range. The band logic and control logic circuitry also determine the leading zero suppression, decimal point and range indications on the display.

3-63. Pre-scaler Circuitry (See Figure 3-10). The 7.75 to 16 MHz signal from the divider chain of the frequency generation circuitry is amplified by A8A3A4Q1 and applied to the pre-scaler frequency divider (A8A3A4IC1 through IC3), which divides by multiples of 2. The frequency divider $F_o/2$ output is applied directly to the output selector logic (A8A3A4IC11). All other frequency divider outputs ($F_o/8$, $F_o/16$, $F_o/32$ and $F_o/64$) are applied to the pre-scaled frequency selector logic (A8A3A4IC7) during internal count operation. This logic controls the pre-scaled frequency output (f_c) as a function of the f_c gate commands from the control logic circuitry (paragraph 3-78). (The control logic circuitry is, in turn, controlled by the frequency RANGE MHz selector and the band logic circuitry.). The resulting output from the pre-scaled frequency selector logic is applied to the output selector logic. In the normal count mode, the LOOP MODE command from the time base generator circuitry (paragraph 3-74) is a logic ONE level. This causes the output from the pre-scaled frequency selector logic to be selected as the F_c output. Similarly, in the frequency lock mode, the LOOP MODE is a logic ZERO level.

3-64. The external count input signal is amplified by A8A3A4Q2 through Q4, shaped by A8A3A4IC5, and applied to the internal/external count selector logic (A8A3A4IC4). When the front-panel EXT COUNT switch is pressed, the "C" gate from the band logic circuitry (paragraph 3-77) is a logical ONE level. This causes the external signal to be applied to the pre-scaled selector logic, instead of the frequency divider $F_o/64$ output. Since the $\overline{A} \cdot \overline{B}$ f_c gate command is also a logic ONE when external count operation is selected, the external signal is selected by A8A3A4IC7 and applied to the output selector logic. Thus, in the normal count mode, the external signal is selected by A8A3A4IC11 as the f_c output. The internal/external selector logic also applies a disabling input to the frequency divider, when the external count mode is selected.

3-65. Counter/Storage Circuitry (See Figure 3-11). This circuitry consists of 6 BCD up/down decade counters (A8A3A3IC1 through IC6) and associated quad storage bistable latches (A8A3A3IC7 through IC12), counter/storage logic circuits (A3A3A3IC14 through IC17), and a zero count logic circuit (A8A3A3IC18 and IC19). The counter/storage circuitry counts up during normal (unlock) operation, and down during frequency lock operation as described below.

3-66. During normal count operation, the UPGATE (ΔT) command from the time base generator circuitry (paragraph 3-74) is a logic ONE level. This allows the decade counters to count the f_c pulses from the pre-scaler circuitry (paragraph 3-63) for the duration of the UPGATE command. At the end of the ΔT period, a STORE command from the time base generator causes the count to be loaded into the storage latches. The time base generator then sends a CLEAR command to the decade counters, resetting them to zero. The BCD outputs from the storage latches are applied to the display circuitry (paragraph 3-64) when the count is transferred to the latches. During normal count operation, the zero count logic circuit is disabled by the LOOP MODE input (which is a logic ONE level at this time) from the time base generator.

3-67. During frequency lock operation, the frequency lock circuitry (paragraph 3-79) is enabled, causing the time base generator to send an active DOWNGATE command (logical ONE level) to the decade counter. This, in turn, causes the counters to count down. When all the counters arrive at zero, the zero count logic circuit generates a LOAD command (as described below) that pre-sets all the counters to the number that is retained in the storage latches (and displayed on the LED display).

3-68. The zero count logic circuit is activated during the frequency lock mode as follows. The BCD outputs from each counter (except the least significant bit of counter IC1) are applied to an associated zero gate logic circuit (IC14, IC15 or IC16). The outputs of this circuit are, in turn, applied to an 8-input NAND gate (IC17), together with the least significant bit of IC1 and F_c pulses. When the LOOP MODE input and all the outputs from the counters are a logical ZERO level, the zero logic gate outputs are all a logical ONE level. When the F_c pulse and the least significant bit are a logical ONE level, the output from the 8-input NAND gate switches to ZERO, clearing D-type flip-flop IC19. At the next cycle of the F_c pulse, the least significant bit is a logical ZERO level. This results in the D-type flip-flop being clocked by the positive output of a gate circuit in IC13. The Q output from the flip-flop drives one-shot multivibrator IC18, which then produces the ZERO pulse output for the frequency lock circuitry. The $\overline{Q}$ output from the D-type flip-flop is the LOAD command that pre-sets the counters with the stored number.

3-69. Display Circuitry (See Figure 3-12). This circuitry is principally composed of six BCD-to-7 segment decoders (A8A3A2IC2, IC4, IC6, IC8, IC10 and IC12) that drive six LED 7-segment displays (A8A3A2IC1, IC3, IC5, IC7, IC9 and IC11). The BCD signals from the counter/storage circuitry (paragraph 3-65) are applied to the decoders, where they are converted to 7-line outputs (a through g). Table 3-2 is a typical truth table for a 7-segment decoder.

TABLE 3-2. BCD INPUT VERSUS DECODER OUTPUT TRUTH TABLE

BCD INPUT				DECODER OUTPUT*							READ
A	B	C	D	a	b	c	d	e	f	g	OUT
0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	0	1	0	0	1	1	1	1	1
0	1	0	0	0	0	1	0	0	1	0	2
1	1	0	0	0	0	0	0	1	1	0	3
0	0	1	0	1	0	0	1	1	0	0	4
1	0	1	0	0	1	0	0	1	0	0	5
0	1	1	0	1	1	0	0	0	0	0	6
1	1	1	0	0	0	0	1	1	1	1	7
0	0	0	1	0	0	0	0	0	0	0	8
1	0	0	1	0	0	0	1	1	0	0	9

* 0 represents the low decoder output state when current flows in the LED segment.

3-70. The proper location for the decimal point is obtained either by applying the appropriate logic signal (2DP, 3DP,

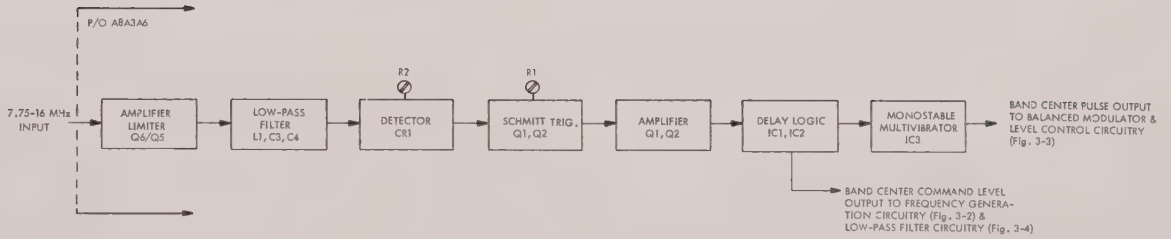
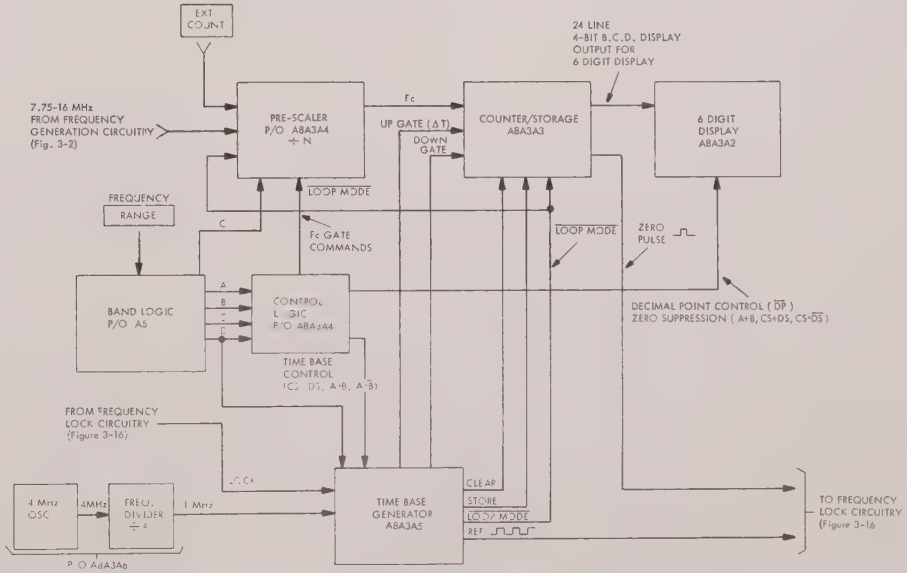
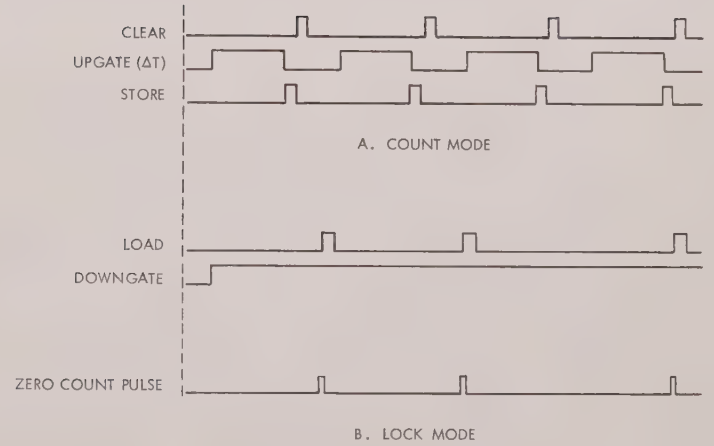


Figure 3-7. Band Center Command Circuitry, Detailed Block Diagram



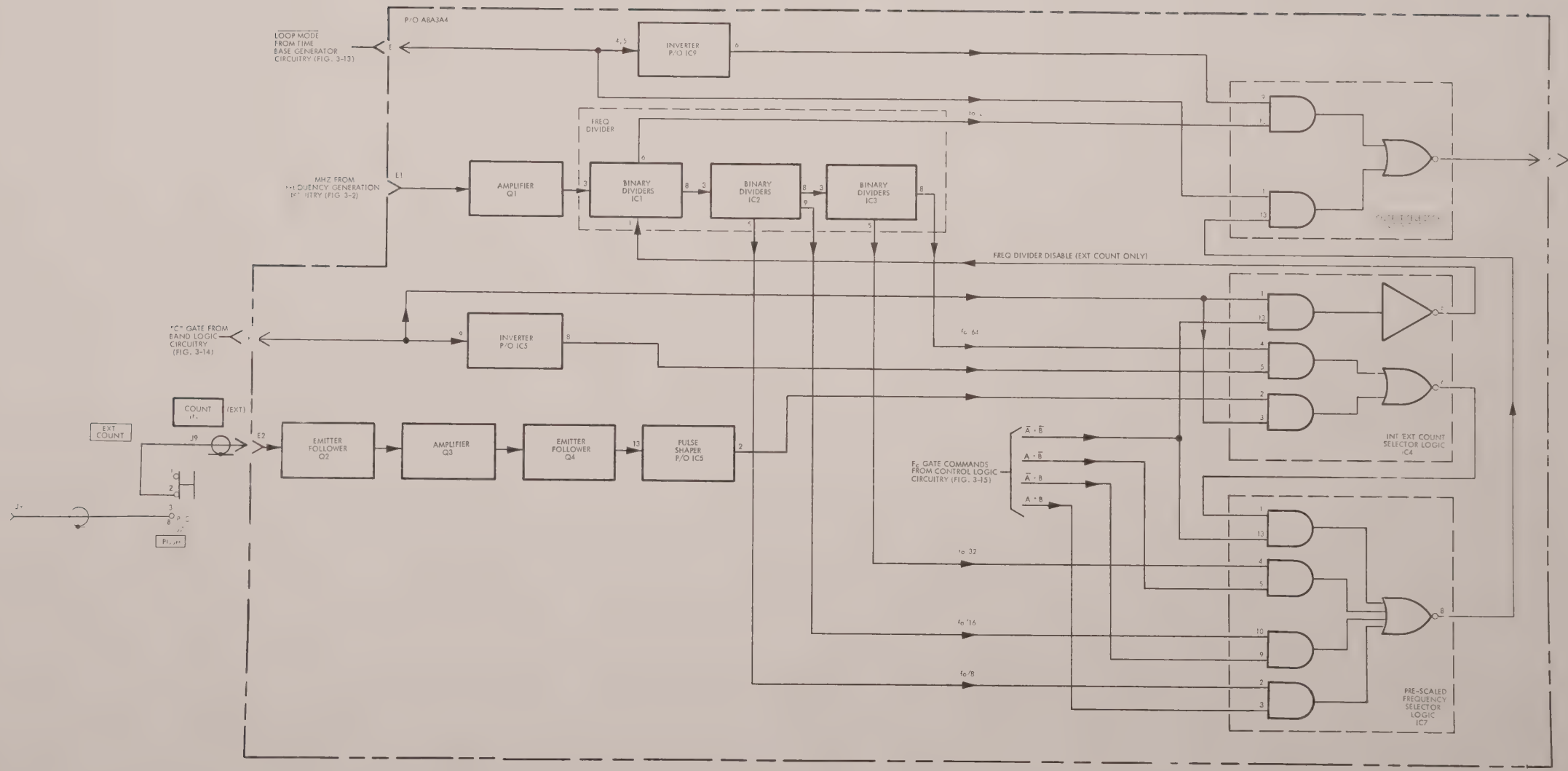
3-8

Figure 3-8. Frequency Counter, Block Diagram



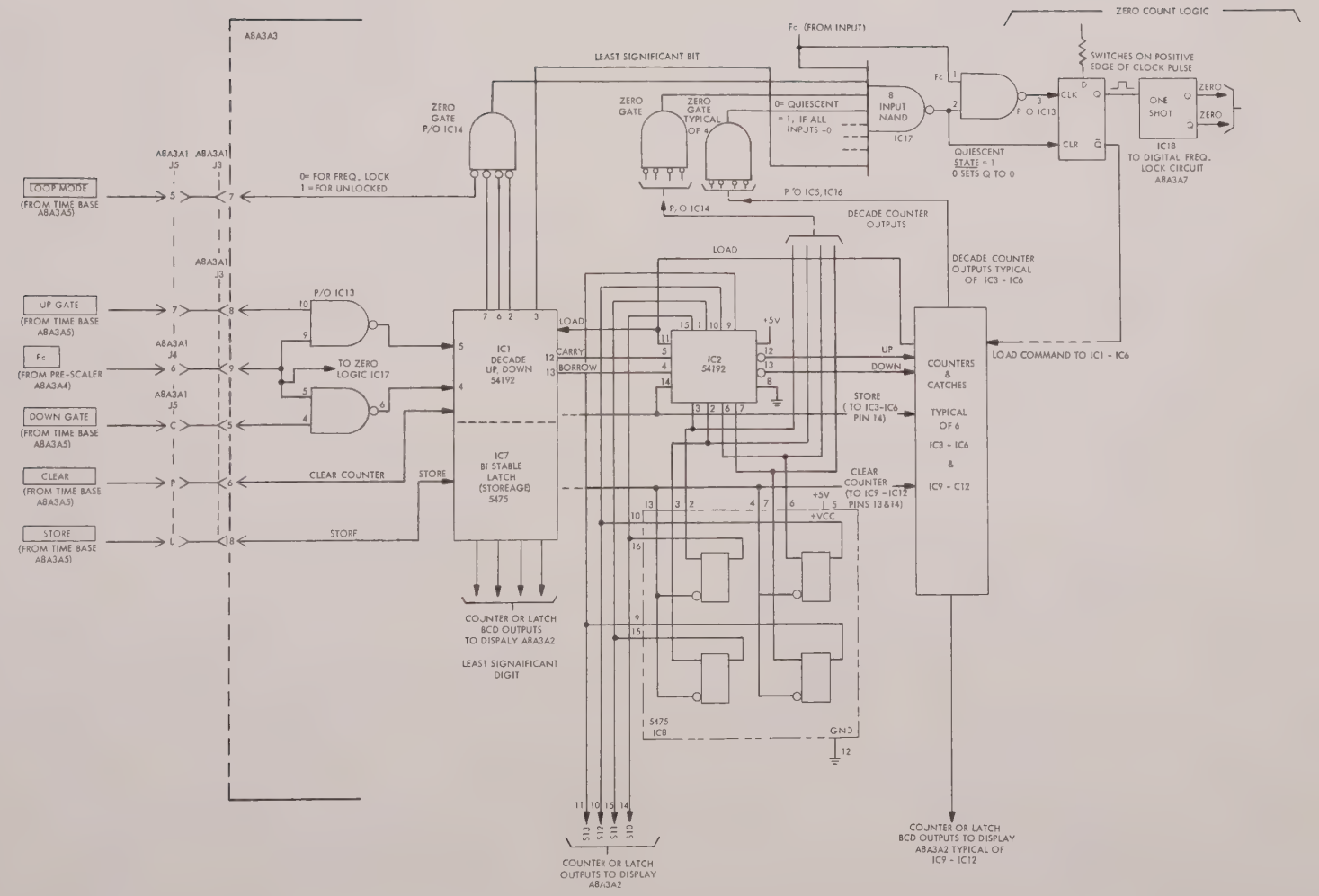
3-9

Figure 3-9. Frequency Counter Count Mode and Lock Mode, Timing Sequences



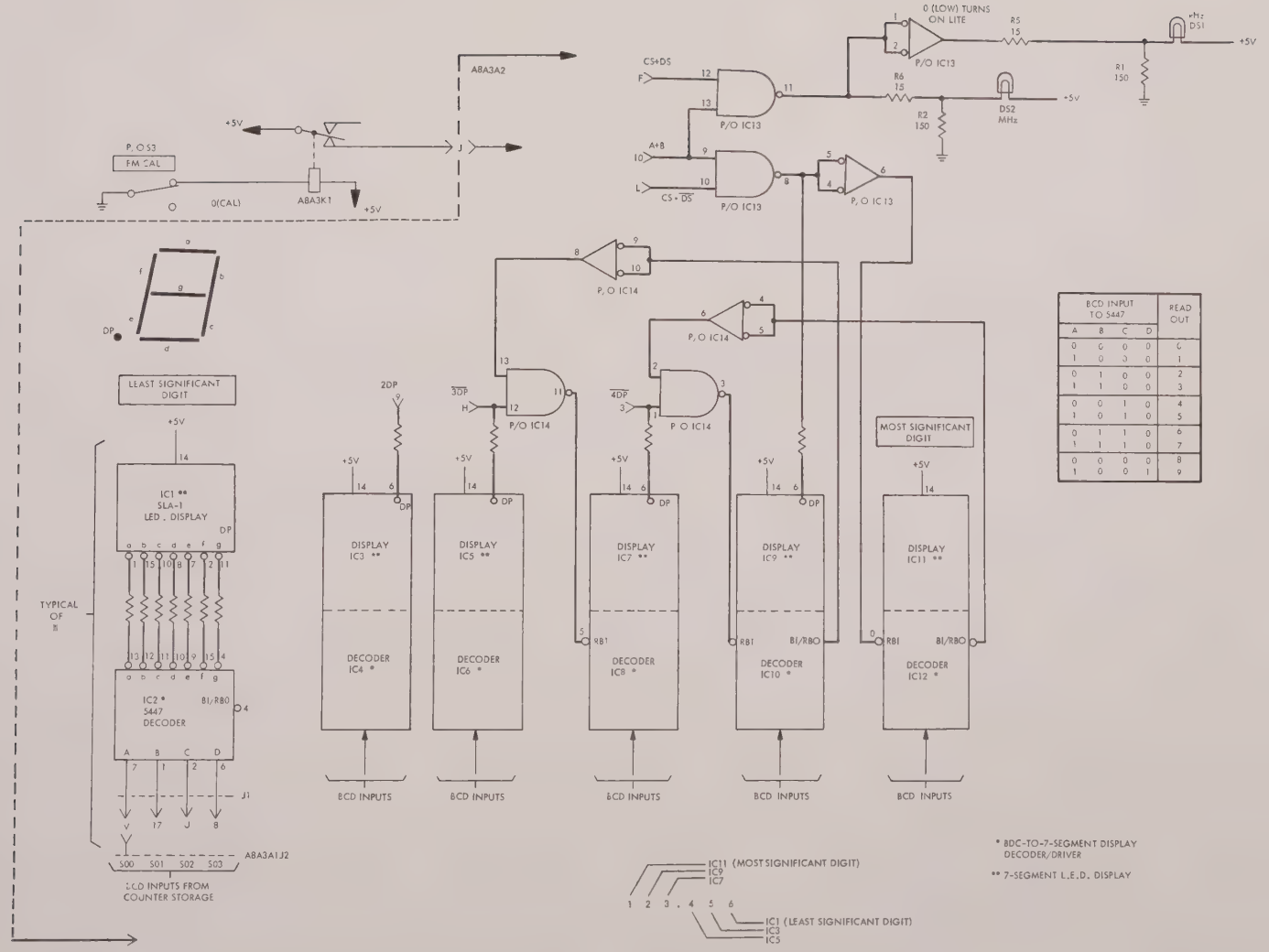
3-10

Figure 3-10. Pre-Scaler Circuitry, Detailed Block Diagram



3-11

Figure 3-11. Counter/Storage Circuitry, Detailed Block Diagram



BCD INPUT TO 5447				READ OUT
A	B	C	D	
0	0	0	0	0
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5
0	1	1	0	6
1	1	1	0	7
0	0	0	0	8
1	0	0	1	9

Figure 3-12. Display Circuitry, Detailed Block Diagram

or $\overline{4DP}$) from the control logic circuitry (paragraph 3-78) directly to the DP terminal of the corresponding decoder (IC3, IC5, or IC7); or by applying the A + B and CS • $\overline{DS}$ logic signals (which both must be a logical ONE level) from the control logic circuitry to the DP terminal of IC9, via a NAND gate IC13. In either case, a logical ZERO level is required at the DP terminal to obtain a decimal point on the display. The display logic circuitry (IC13 and IC14) performs two other functions: it suppresses leading zeros, as necessary; and it controls the lighting of the proper range indicator (MHz or kHz). Both of these functions are described below.

3-71. The zero suppression logic functions as follows. If the most significant digit is zero, the A + B and CS • $\overline{DS}$ inputs cause the output of the NAND gate in IC13 to be a logical ONE level. This, in turn, causes the holding off of a decimal point at the second most significant display (IC9); and the suppression of a zero indication at the most significant display (IC11), by way of an inverter in IC13. In a similar manner, the output at the B1/RBO terminal of IC10 or IC12 is gated with the $\overline{3\ DP}$ or $\overline{4\ DP}$ logic signal, respectively, to suppress the zero indication at IC8 or IC10, when necessary.

3-72. The illumination of the MHz and kHz indicators (DS2 and DS1, respectively) is controlled by a NAND gate in IC13. When the CS + DS and A + B logic signals are both a logical ONE level, a logical ZERO level is applied to the MHz indicator, causing it to illuminate. At the same time, an inverter in IC13 causes a ONE level to be applied to the kHz indicator, keeping it turned off. When either of the input to the NAND gate is a logical ZERO level, the kHz indicator illuminates and the MHz indicator turns off.

3-73. When FM CAL pushbutton S3 is pressed, ground is removed from relay A8A3K1, causing it to de-energize. With A8A3K1 de-energized, +5 volts is removed from the three most significant display (IC7, IC9 and IC11) and the MHz and kHz indicators. Thus, during FM peak sensitivity calibration, only the three least significant displays (IC1, IC3 and IC5) are illuminated.

3-74. Time Base Generator Circuitry (See Figure 3-13). This circuitry comprises an internal 1 MHz oscillator, a frequency divider, and time base logic circuits. The 1 MHz oscillator includes a 4 MHz stable oscillator (A8A3A6Q8) whose output is converted to a 1 MHz signal by a divide-by-four frequency divider (A8A3A6IC4). Either the internal 1 MHz signal or an external 1 MHz signal applied to rear-panel 1 MHz IN connector J8 is processed by the frequency divider in A8A3A5, as determined by the setting of TIME BASE switch S2. The frequency divider essentially consists of two parts. The first portion comprises a series/parallel divider chain that provides a 15.625 kHz signal and three selectable signals to a B multiplexer in A8A3A5IC10. The frequencies of the three signals are primarily determined by either logical OR functions or an A multiplexer in IC10 as a function of the logic inputs from the band logic circuitry (paragraph 3-77) and the control logic circuitry (paragraph 3-78). The B multiplexer output (2Y), which is selected as a function of logic inputs from the control logic circuitry, is then simultaneously applied to the second portion of the frequency divider and the time base logic circuits.

3-75. The 2Y signal output from the B multiplexer is divided-by-8000 by the remainder of the frequency divider, resulting in the UPGATE (ΔT) command pulse output (refer to Table 3-3) from the time base generator circuitry. During the frequency lock mode, an input from the frequency lock circuitry (paragraph 3-79) disables this output, by way of a D-type flip-flop in IC15 and a NAND gate in IC4.

TABLE 3-3. ΔT GATE GENERATION DATA

Range MHz Switch Setting	Logic Input					ΔT Gate Time
	D	A+B	A•B	CS	DS	
248 - 512 MHz 124 - 256 MHz 62 - 128 MHz 31 - 64 MHz	1	1	0	1	1	256 msec
15.5 - 32 MHz 7.75 - 1 MHz	1	1	0	0*	1	320 msec*
External Count						
0 - 9999.99 kHz (0.1 sec time base)	0	0	1	1	0	100 msec
0 - 9999.99 kHz (1 sec time base)	1	0	1	0	0	1000 msec

* CS is a logical 1 level during FM calibration, thereby resulting in a 256 msec ΔT gate for bands 1 through 6 in normal internal count mode.

3-76. The time base logic circuit consists of two divide-by-two stages in IC15, two D-type flip-flops, and associated AND gate logic (NAND gate followed by an inverter). The other branch of the 2Y output from the B multiplexer is used as a clock pulse by the time base logic circuits for the generation of STORE, CLEAR DOWNGATE and $\overline{\text{LOOP MODE}}$ outputs. The DOWNGATE command and an active $\overline{\text{LOOP MODE}}$ logic level are only generated during the frequency lock mode from the LOCK level input from the frequency lock circuitry. At this time, the active $\overline{\text{LOOP MODE}}$ level causes the reference square wave for the frequency lock circuitry to be produced at the output of a NAND gate in IC17 and the STORE and CLEAR outputs to be disabled via two NAND gates in IC16.

3-77. Band Logic Circuitry (See Figure 3-14). This circuitry consists primarily of four two-input NOR gates in A5A3IC2. When a ground (logical ZERO level) is provided to either input of these gates, a logical ONE level output (+5V nominally) is obtained. When ground is removed from both inputs, the +5V supply provides logical ONE level inputs (through two resistors) to a gate, resulting in a logical ZERO output. In the normal internal count mode, the RANGE MHz selector switch contacts (A5A2S1A, S1B; and A5A3S1A, S1B) supply either a ground or open to the NOR gates, resulting in the 4-bit binary code output indicated in Table 3-4. In the external count mode, EXT count switch S7 causes ground to be removed from the contacts of the RANGE MHz selector switch. This, in turn, results in the following inputs to the NOR gates: two logical ONE levels at the A and B NOR gates; a logic ONE level and a logical ZERO level and logical ZERO or ONE level (depending on the position of INT TIME BASE switch S6) at the D NOR gate. The resultant 4-bit binary code output is also indicated in Table 3-4. During FM calibration, FM CAL pushbutton S3 provides a

ground to the four NOR gates, resulting in a ONE level output from the gates regardless of the setting of the RANGE MHz switch.

TABLE 3-4. BAND LOGIC CIRCUITRY OUTPUT DATA

RANGE MHz Switch Setting	Gate Logic Output D	C	B	A
248 - 512 MHz	1	1	1	1
124 - 256 MHz	1	1	1	0*
62 - 128 MHz	1	1	0*	1
31 - 64 MHz	1	0*	1	1
15.5 - 32 MHz	1	0*	1	0*
7.75 - 16 MHz	1	0*	0*	1
External Count				
0 - 9999.99 kHz (0.1 sec time base)	0	1	0	0
0 - 999.999 kHz (1 sec time base)	1	1	0	0

* Logical 1 level during FM calibration

3-78. Control Logic Circuitry (See Figure 3-15). This circuitry provides the necessary logical gating functions to convert the 4-bit binary code signal from the band logic circuitry (paragraph 3-77) into logic signals which control the pre-scaler frequency output (F_c) selection, the time base gate (ΔT) period, and the range indicator and decimal point logic in the display. Table 3-5 lists the gate logic outputs from the control logic circuitry for the normal internal count mode and the external count mode.

3-79. FREQUENCY LOCK CIRCUITRY.

3-80. This circuitry consists of a frequency lock flip-flop and an automatic frequency lock circuit. The circuitry, which is contained on assemblies A5 and A8, is shown in Figure 3-16 and described in the following subparagraphs.

3-81. Frequency Lock Flip-Flop. This stage employs two inverters in A5A3IC2 in a bistable latch configuration. The set input of the flip-flop is connected to an isolation diode (A5A3CR6) and the reset input is connected to a four-input OR gate (A5A3CR3, CR4, CR8 and CR15). Applying a logical ZERO level (ground) to either the set or reset input of the flip-flop places it in the locked or unlocked state, respectively. Both inputs are normally held at a logical ONE level via resistors connected to the +5V supply.

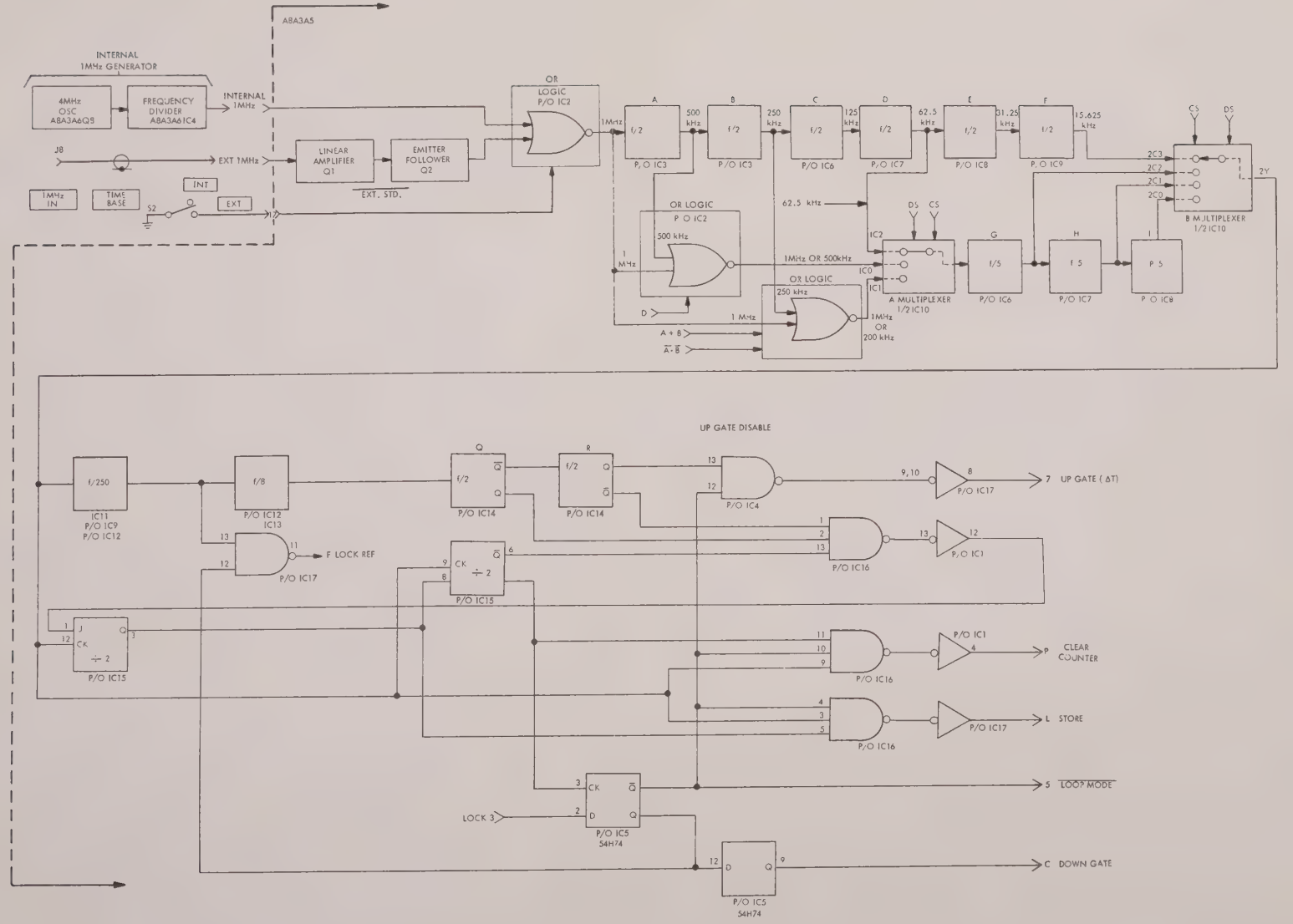
3-82. When the front-panel LOCK/NORMAL switch is momentarily set to the LOCK position, the frequency lock flip-flop is placed in the locked state. This causes the LOCK command to be active (logical ONE level) and the front-panel LOCK indicator (LED) to turn on. Similarly, the flip-flop is placed in the unlocked state when any one of the following conditions occurs: the LOCK/NORMAL switch is momentarily set to the NORMAL position; the front-panel EXT COUNT or FM CAL pushbutton is pressed; the automatic frequency lock circuit is out-of-lock; or the RANGE MHz switch position is changed. Transistor switch A5A5Q1 is normally held at cutoff by a logical ZERO level input (ground) from the wiper arm of A5A5S1-B; whenever the RANGE MHz switch position is changed, ground is momentarily removed from the switch contact. This causes A5A5Q1 to momentarily conduct, applying a logical ZERO level to the reset input of the flip-flop.

3-83. Automatic Frequency Lock Circuit. This circuit is principally composed of lock ramp integrator A8A3A7Q3, Q5; zero pulse sample switch A8A3A7Q4; buffer amplifier A8A3A7Q7; sample and hold stage A8A3A7Q6; and control logic in A8A3A7U1. When frequency lock flip-flop A5A3IC2 is placed in the locked state, a logic ONE level is applied to the lock control logic (D-type flip-flop) in A8A3A7U1. This, in turn, causes lock/unlock switch Q2 to be turned off (via driver Q1), thereby disabling the front-panel VERNIER frequency control. At this time, the stable reference square wave from the time base generator (paragraph 3-77) is applied to the lock ramp integrator, where it is converted to a -5V to -15V triangular wave. The stable triangular wave is applied to zero pulse sample switch Q4, together with the ZERO count pulse from the counter/storage circuitry (paragraph 3-63). Each ZERO count pulse turns on Q4, and the sampled output from Q4 is stored and held by capacitor C5 of sample and hold stage Q6 until the application of the next ZERO pulse. If the master oscillator frequency is constant, the instantaneous voltage will be equal to the stored voltage, which will not change. If the frequency drifts, the stored voltage will change. The stored voltage is applied to the master oscillator via the modulation selection and AM/FM metering circuitry. Voltage changes are in the proper direction to change the frequency back to the original frequency. Gain around the circuit is sufficient to keep the master oscillator locked to the stable reference square wave. Figure 3-17 shows the timing of the automatic frequency lock circuit.

3-84. If the master oscillator goes out of the lock capture range during the frequency lock mode, frequency lock flip-flop A6A3IC2 is placed in the unlocked state as follows. The out-of-lock control logic (D-type flip-flop) in A8A3A7 is applied two inputs: the stable reference square wave and the ZERO count pulse. When the master oscillator frequency is in the lock capture range, the ZERO pulse always occurs while the reference square wave is a logical ONE level. However, when the master oscillator frequency drifts out of the capture range, the ZERO pulse occurs while the reference square wave is a logical ZERO level. This results in a pulse output from the out-of-lock logic which places the frequency lock flip-flop in the unlocked state. Whenever this flip-flop is in the unlocked state, a logical ZERO level is applied to the lock control logic, turning on lock/unlock switch Q2. This, in turn, connects the VERNIER frequency control to the input of the sample and hold stage, thereby allowing vernier control to the master oscillator frequency.

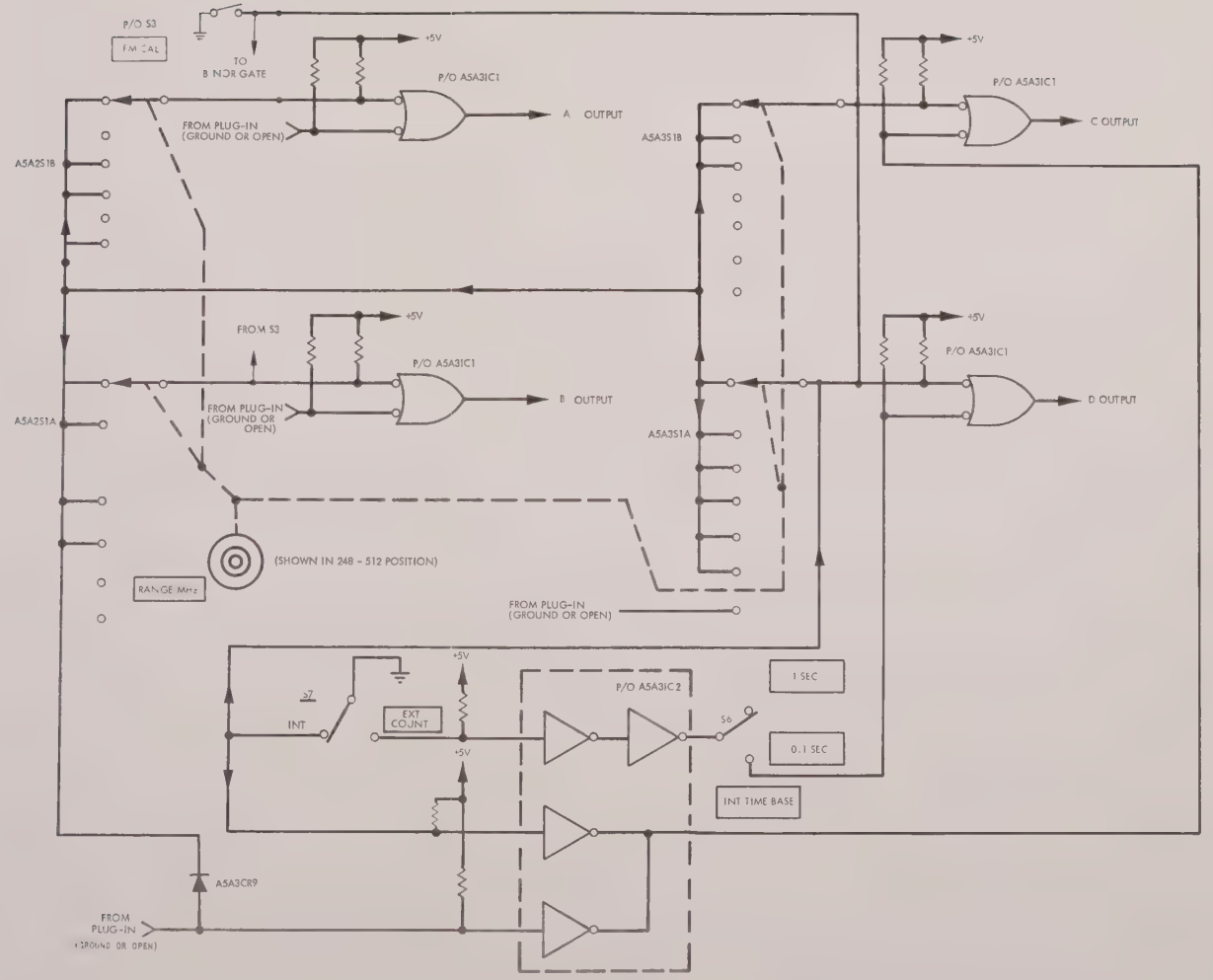
3-85. REGULATED POWER SUPPLIES.

3-86. The regulated power supplie (Figure 3-18) consist of input circuitry, three unregulated power supplies and five voltage regulators. Each of these is discussed in the following subparagraphs.



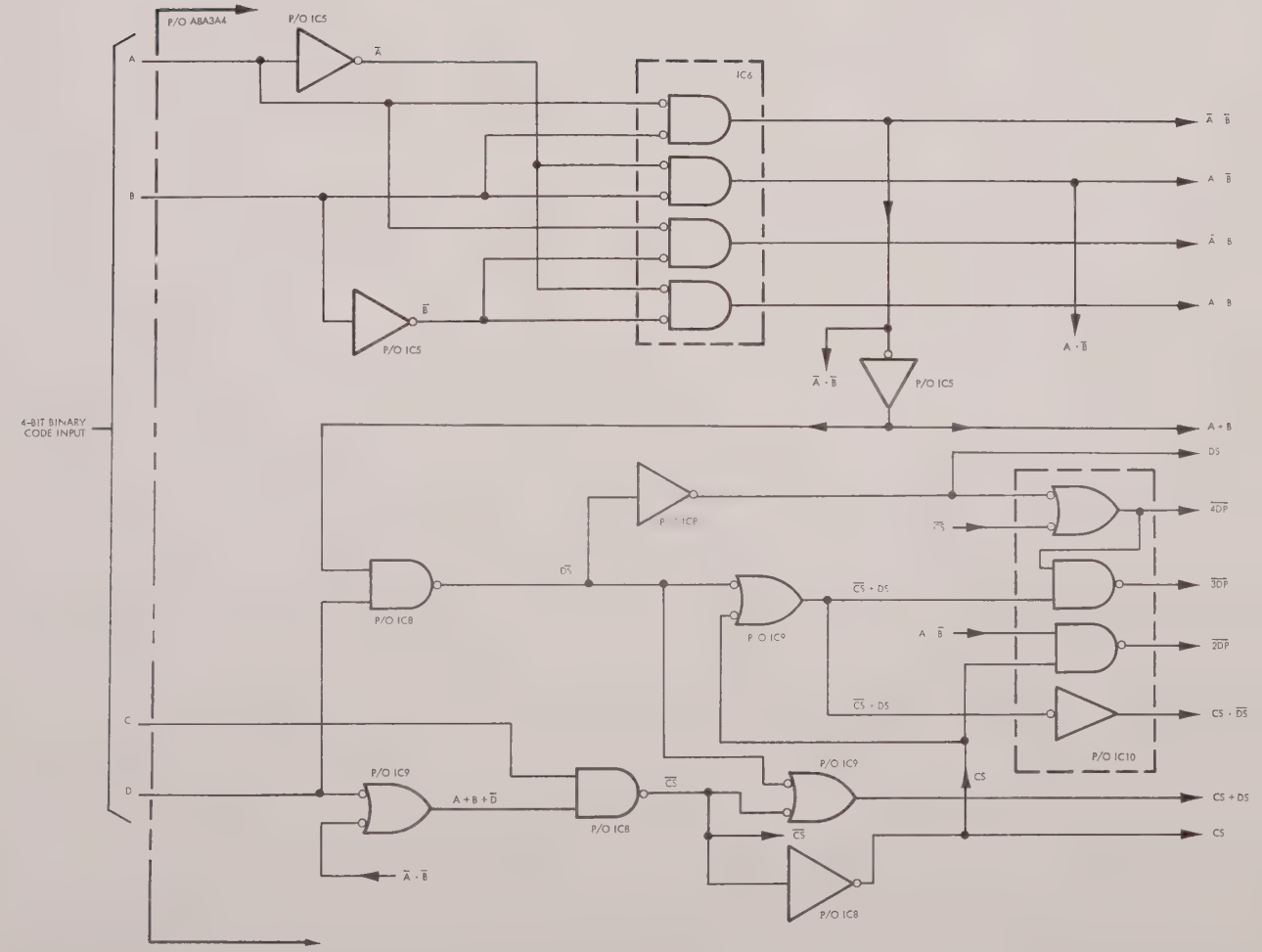
3-13

Figure 3-13. Time Base Generator Circuitry, Detailed Block Diagram



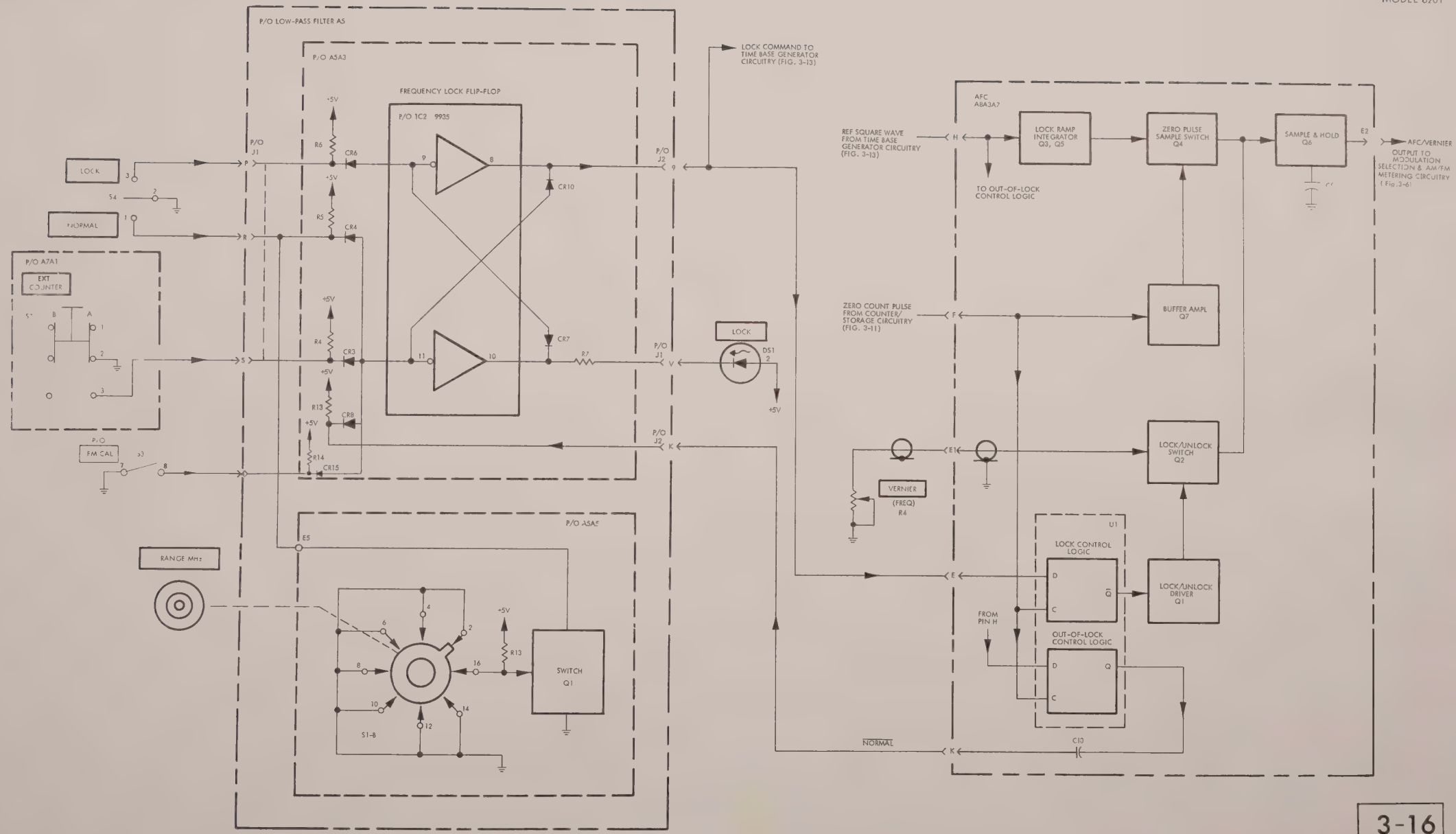
3-14

Figure 3-14. Band Logic Circuitry, Simplified Logic Diagram



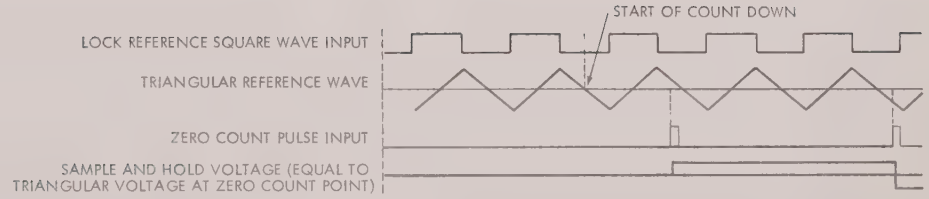
3-15

Figure 3-15. Control Logic Circuitry, Detailed Logic Diagram



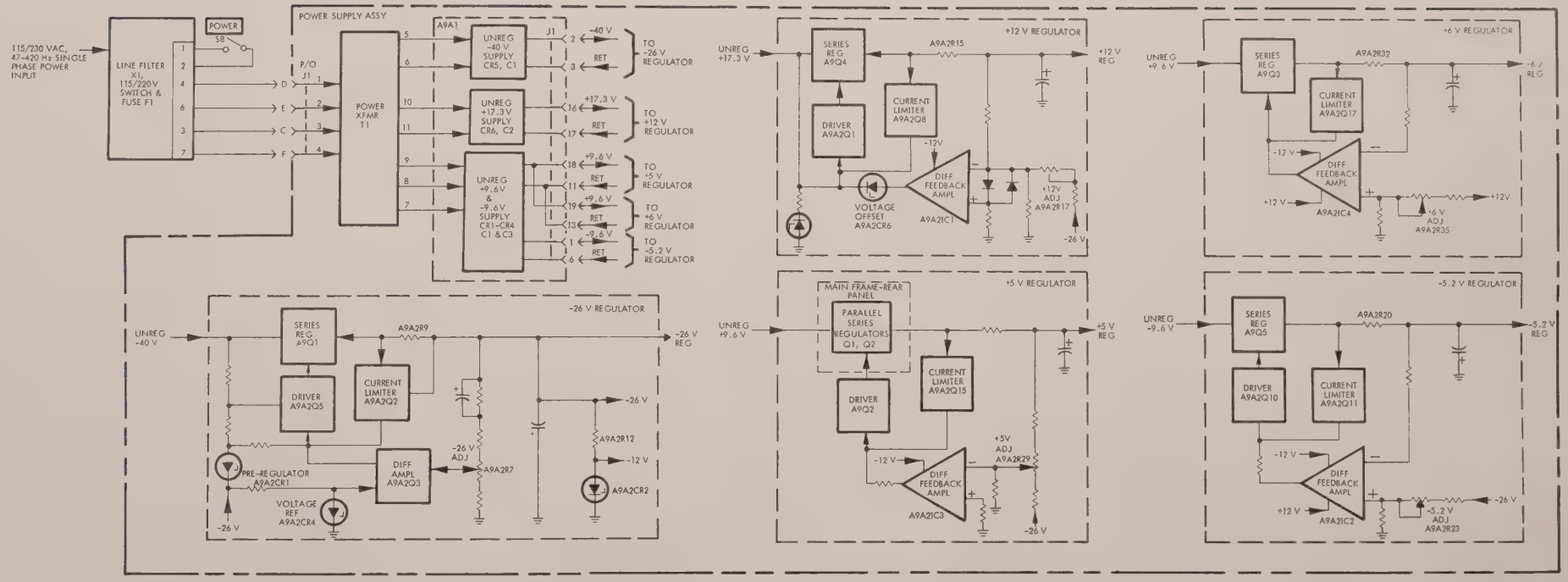
3-16

Figure 3-16. Frequency Lock Circuitry, Detailed Block Diagram



3-17

Figure 3-17. Automatic Frequency Lock Circuit, Timing Diagram



3-18

Figure 3-18. Regulated Power Supplies, Detailed Block Diagram

3-87. Input Circuitry. The input circuitry comprises line filter X1, a 115/230V selector switch, fuse F1 and power transformer T1. When front-panel POWER push-button S8 is pressed, 115 or 230 VAC, 47 to 420 Hz single-phase line power is applied through the line filter (which provides RFI protection) and the power transformer to the unregulated power supplies. The 115/230V selector switch connects the two input windings of T1 either in parallel or series for a line power of 115 VAC or 230 VAC, respectively. Depending on the input power, fuse F1 has a current rating of 1 ampere (115 VAC) or 0.5 ampere (230 VAC).

3-88. Unregulated Power Supplies. With the exception of the +9.6V and -9.6V unregulated power supply, the unregulated supplies (-40V and +17.3V) consist of a full-wave bridge rectifier and an output filter capacitor. The +9.6V and -9.6V unregulated power supply contains a full-wave bridge rectifier and two output filter capacitors connected in series to obtain the +9.6V and -9.6V outputs.

3-89. Voltage Regulators. Each of these circuits is essentially a conventional series regulated supply (consisting of a difference amplifier, driver and pass transistor) with output current overload protection. Screwdriver adjustments are provided to set the output levels of the regulators.

TABLE 3-5. CONTROL LOGIC CIRCUITRY OUTPUT DATA

RANGE MHz Switch Setting	Gate Logic Output											
	$\overline{A} \cdot \overline{B}$	$A \cdot \overline{B}$	$\overline{A} \cdot B$	$A \cdot B$	$A + B$	DS*	CS**	$CS \cdot \overline{DS}$	$CS + DS$	$\overline{2DP}$	$\overline{3DP}$	$\overline{4DP}$
248 - 512 MHz	0	0	0	1	1	1	1	0	1	1	0	1
124 - 256 MHz	0	0	1	0	1	1	1	0	1	1	0	1
62 - 128 MHz	0	1	0	0	1	1	1	0	1	1	0	1
31 - 64 MHz	0	0	0	1	1	1	0	0	1	1	1	0
15.5 - 32 MHz	0	0	1	0	1	1	0	0	1	1	1	0
7.75 - 16 MHz	0	1	0	0	1	1	0	0	1	1	1	0
31 - 64 MHz ***	0	0	0	1	1	1	1	0	1	1	0	1
15.5 - 32 MHz ***	0	0	1	0	1	1	1	0	1	1	0	1
7.75 - 16 MHz ***	0	1	0	0	1	1	1	0	1	1	0	1
External Count												
0 - 9999.99 kHz (0.1 sec time base)	1	0	0	0	0	0	1	1	1	0	1	1
0 - 999.999 kHz (1 sec time base)	1	0	0	0	0	0	0	0	0	1	0	1

*$DS = (A + B + \overline{D}) \cdot D = (A + B) \cdot D$

**$CS = (A + B + \overline{D}) \cdot C$

***During FM calibration

TABLE 3-6. GENERAL CIRCUIT THEORY.

1. Singer Instruments are formed, principally, of standard semiconductor circuits which are in common use. A few special circuits are used repeatedly. These two classes of circuits are described in detail immediately hereafter. Some special circuits are used once or twice only. These circuits are described in detail, in Section IV, when the detailed circuit descriptions, in order of signal flow, reach those particular circuits.

2. STANDARD CIRCUITS.

3. The circuits in Figure 1 use PNP (circuit A) and NPN (circuit B) transistors to convert low-level low-impedance signals to high-level high-impedance signals at higher levels of power. Signals into the input of each circuit cause current to flow in the input resistors. As the input voltage goes

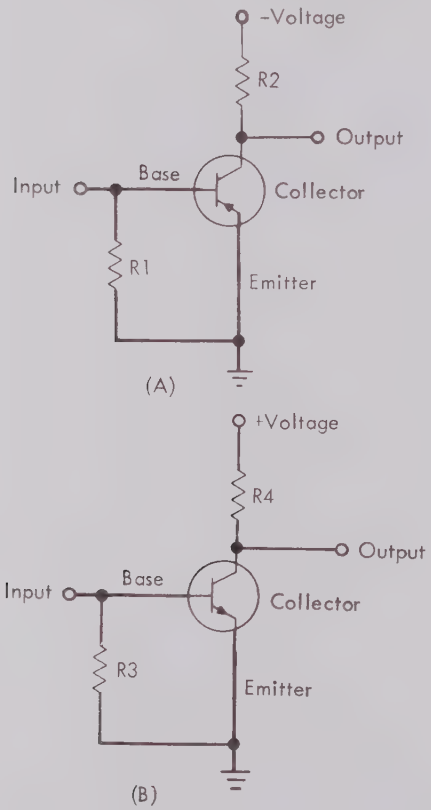


Figure 1. Common Emitter Amplifiers

negative (A) or positive (B), current flows in the base of the transistor. This allows current to flow between collector and emitter, in an amount equal to B times the base current. The collector current causes voltage drop across the collector resistor. The collector offers high impedance to current flow (a large change in collector-emitter voltage causes only a small change in collector current). Hence

$$E_C = B\, i_b\, R_C$$

Where E_C = Voltage across Collector Resistor, R_C

B = Current Gain of Transistor

i_b = Current in Base of Transistor

For low impedance into the base (usually around 1 kΩ) and high impedance at the collector, possible power gain is usually 25 dB to 40 dB or more. Polarity of the voltage changes are, of course, reversed from base to collector. These circuits will be called common emitter amplifiers.

4. The two circuits in Figure 2 use PNP (circuit A) and NPN (circuit B) transistors to convert medium-to-high level medium-impedance signals to medium-to-high level low-impedance signals at higher levels of power. The base of

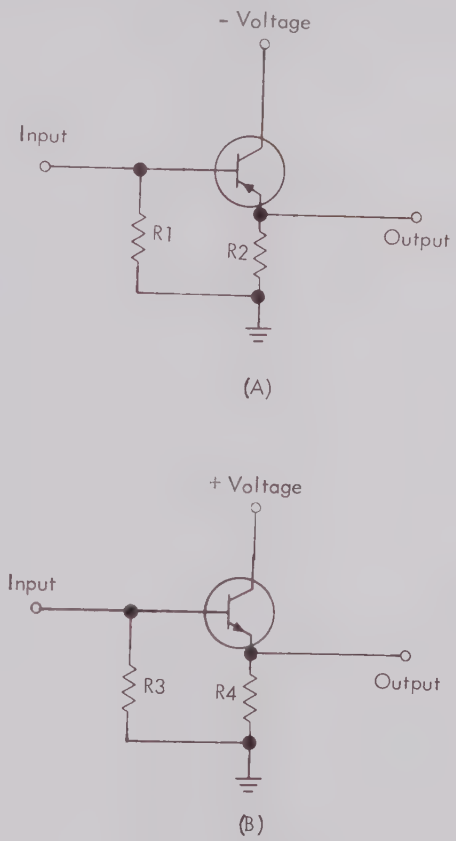


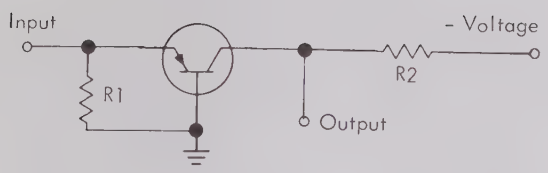
Figure 2. Emitter-Follower Amplifiers

of each transistor offers an impedance-to-input of B times the emitter resistor value, plus approximately 1 kΩ. Current in the emitter is equal to the base current times (B+1), the B representing collector current, the "1" representing base current. Impedance level of the emitter is equal to impedance of the circuit driving the input divided by (B+1).

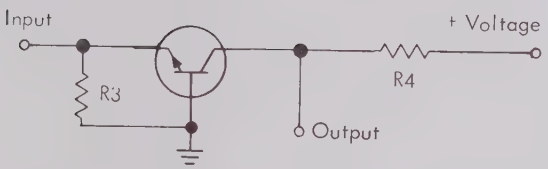
5. In this circuit there is a slight loss of voltage variation, from input to output. Possible power gain is usually from 20 dB to 30 dB. These circuits will be called emitter followers.

6. The two circuits in Figure 3 use PNP (circuit A) and NPN (circuit B) transistors to convert currents from a low impedance source to currents of almost the same value into a high impedance load.

TABLE 3-6. GENERAL CIRCUIT THEORY (CONTINUED)



(A)



(B)

Figure 3. Common Base Amplifier

Current in the emitter of either transistor splits between the base and the collector. The relation is the same as before.

$$I_c = B\, i_b$$

$$I_e = (B+1)\, i_b$$

Since the collector impedance is high, the load impedance can be high. Power out is equal to $I\ R_{out}$. Emitter impedance is low (approximately $1\ \Omega \div [B+1]$). Power in is equal to $I_e^2\, R_{in}$.

7. Power Gain G_p is:

$$G_p = \frac{I_c^2\, R_{out}}{I_e^2\, R_{in}}$$

$$= \frac{(Bi_b)^2\, R_{out}}{[(B+1)\, i_b]^2\, \frac{1\ k\Omega}{(B+1)}}$$

$$= \frac{(B+1)(Bi_b)^2\, R_{out}}{(B+1)^2\, i_b^2 \cdot 1\ k\Omega}$$

$$= \frac{B^2\, R_{out}}{(B+1)\ 1\ k\Omega}$$

Since B+1 is only slightly larger than B, assuming B = 50 or more, which is common,

$$G_p \approx \frac{R_{out} \cdot B}{1\ k\Omega}$$

Since the collector impedance is generally from 20 k Ω to 100 k Ω,

$$G_p \approx \frac{60\ k\Omega \cdot B}{1\ k\Omega} = 3{,}000 = 35\ dB$$

Usual power gain is 10 dB to 20 dB. This circuit is usually used to obtain higher frequency response in an amplifier. It will be called a common base amplifier.

8. TWO-STAGE AMPLIFIERS.

9. The circuits described in this section contain two stages of amplification, using the circuits described in Section 2. Circuits may be direct coupled, capacitor coupled, or transformer coupled.

10. The circuit in Figure 4 has in it two common emitter circuits, capacitor coupled.

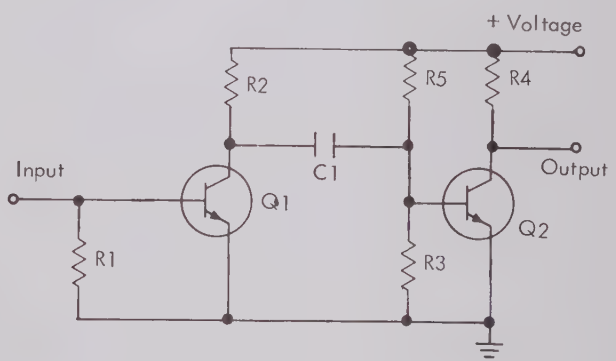


Figure 4. Two-Stage Capacitor-Coupled Amplifier

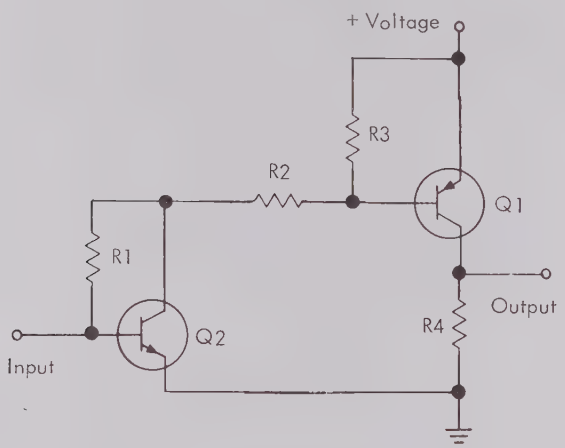
Resistor R5 is added to provide bias to Q2 so that Q2 will not normally be cut off. R3 is often not used in the circuit, since it puts additional load on the output of Q1.

11. Another bias variation connects the top of R5 to the output rather than to + voltage. Since output voltage changes are of opposite polarity to input voltage changes, this is a negative feedback path which tends to maintain constant collector current in Q2. This gives automatic bias correction for changes in supply voltage and in temperature. Input impedance to Q2 is lowered, which reduces overall gain, generally by about 3 dB. Capacitor C1 disconnects the direct voltage of the Q1 collector from the base of Q2 so that the biasing described above may be achieved. This circuit will be called a two-stage capacitor coupled cascade amplifier.

12. The circuit, as shown, has a power gain, usually, of 40 dB to 60 dB. The loss of gain below twice that shown for each simple amplifier is due to the low impedance (1 k Ω) load presented to the collector of Q1 by the base of Q2.

TABLE 3-6. GENERAL CIRCUIT THEORY (CONTINUED)

13. The circuit in Figure 5 uses one PNP (Q1) and one NPN (Q2) transistor in a two-stage direct coupled amplifier.



Fiaure 5. Two-Stage Direct-Coupled Amplifier

The input current varies the current to the base of Q2. Current is normally supplied through R1, which maintains a constant current in the collector of Q2. This feedback current, however, is not sufficient to cancel the effect of the input current. For this automatic bias circuit, the collector current change is about 70% of what it would be if fixed bias was provided. R2 provides voltage changes at the collector of Q2 so that automatic bias in R3 bypasses part of the collector current from Q2 so that it does not go to the base of Q1. Since current into the base of Q1 varies as the square of the voltage across R3, R3 can be selected so that more than half the collector current of Q2 flows through R3, but more than 70% of the changes in the collector current of Q2 occur in the base current of Q1.

14. Changes in the collector current of Q1 are equal to B times changes in base current. The current gain through the whole circuit:

$$G_I \approx B_2 \cdot 0.7 \cdot 0.7 \cdot B_1$$

$$= 0.5\, B_1 B_2$$

Input impedance to Q2 is about 800Ω, considering effect of feedback. Assuming a 1 kΩ load, R4 power gain is:

$$G_p = (0.5\, B_1 B_2)^2 \frac{1\,k\Omega}{800\,k\Omega} =$$

For $B_1 = B_2 = 60$,

$$G_p = (0.5 \cdot 60 \cdot 60)^2\, 25 = 4{,}050{,}000 = 66\ dB$$

This is a common figure for the power gain of this type of circuit. This circuit will be called a complementary two-stage amplifier.

15. The circuit shown in Figure 6 uses two NPN transistors in common emitter configuration, transformer coupled. DC bias for Q1 is provided by R1 and R2. R5 determines the emitter-current flow for the voltage set by R1 and R2. Direct collector current is usually set at one-half the desired peak current. R3 and R4 provide bias for Q2. R6 determines emitter current flow for Q2. Capacitors C2 and C3 bypass

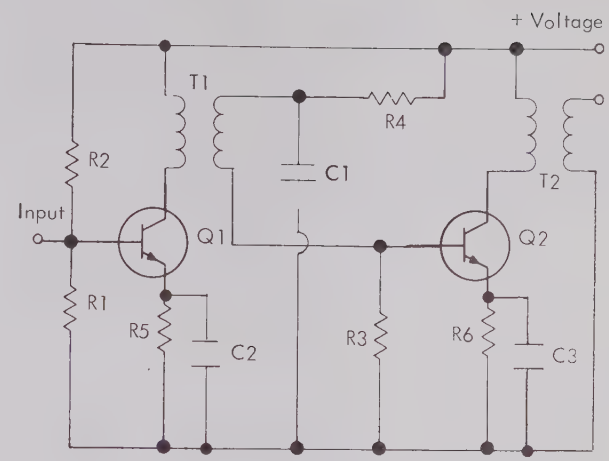


Figure 6. Two-Stage Transformer-Coupled Amplifier

around the emitter resistors so that input impedance (ac) to the transistors is low, hence low power is needed to provide the proper signal current into each base. In each transistor, input signal current times B is equal to collector signal current.

16. The transformer, T1, matches impedance of the collector of Q1 (around 16 kΩ) to the impedance of the base of Q2 (around 1 kΩ). This makes signals current into the base of Q2 four times the collector signal current in Q1. C1 bypasses transformer current to ground so that the load on the transformer is actually 1 kΩ, rather than 1 kΩ plus R4, which is what it would be without C1.

17. From the preceding discussion it is seen that current in the primary of T2 will be:

$$I_{T2} = I_{input}\, B_1 \cdot 4 \cdot B_2$$

For $B_1 = B_2 = 60$,

Current Gain $G_I = 60 \cdot 4 \cdot 60 = 14{,}400$

Assuming 1 kΩ input impedance and 16K impedance at the T2 primary, Power Gain:

$$= G_I^2 \cdot \frac{Z_{out}}{Z_{in}}$$

$$= 14{,}400^2 \quad \frac{16\,K}{1\,K}$$

$$G_p = 207{,}360{,}000 \times 16 = 3{,}717{,}760{,}000$$

$$\approx 96\ dB$$

The secondary of T2 is to be connected to the load. The turns ratio of T2 is to be the ratio required for exact impedance match. It will be seen that insertion of transformers increases the gain of the two-stage complementary amplifier by 30 dB. This is done at the expense of inserting a number of biasing resistors and bypass capacitors, and of eliminating direct current amplification.

TABLE 3-6. GENERAL CIRCUIT THEORY (CONTINUED)

NOTE

Descriptions of multi-transistor amplifiers will be in the general form: For example, "Three-stage, capacitor coupled, plus complementary two-stage, plus emitter follower, amplifier." This means 3 stages of Figure 1A (or B), capacitor coupled as in Figure 4, followed by the circuit of Figure 2A (or B).

18. INTEGRATED CIRCUITS.

19. Several types of integrated circuits are used. They will be treated as single active parts having one or more inputs and one or more outputs. For signal tracing purposes, power supply connections will be ignored except where they are used as signal outputs. These applications will be described in detail in the Circuit Theory text.

20. OPERATIONAL AMPLIFIERS.

a. Operational amplifiers are direct-coupled multi-transistor amplifiers. They have differential inputs and either single or differential output. Current and/or voltage gain is usually from 1,000 to 100,000. Power gain is not especially high because input impedance is usually very high (1 MΩ or more), and output impedance is rather low (about 500 Ω). Assuming:

current gain = G_I = 100,000

input impedances = Z_{in} = 1 MΩ

output impedance = Z_{out} = 500 Ω

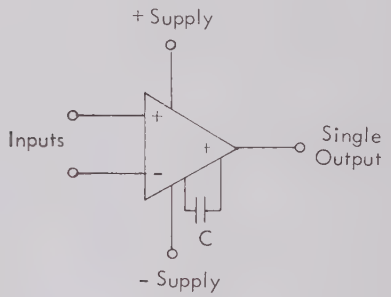
$$\text{Power Gain} = G_p = G_I^2 \frac{Z_{out}}{Z_{in}}$$

$$= (10^5)^2 \frac{500\,\Omega}{10^6\,\Omega}$$

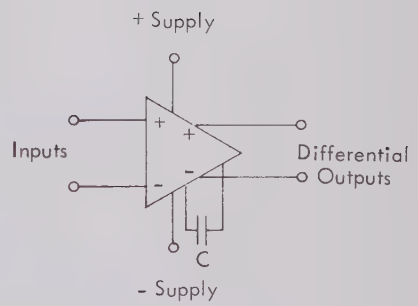
$$G_p = 5 \cdot 10^6 = 67\ \text{dB}$$

This is similar to the gain of a two-stage complementary amplifier.

21. The characteristics which lead to the use of IC operational amplifiers are very high impedance inputs, high rejection of effect of common mode inputs (both differential inputs move in the same direction, over many volts, while the differential voltage only moves a few millivolts), and low phase shift through the circuits so that negative feedback can be used readily without causing oscillations. The symbols used are shown in Figure 7, A and B. In Figure 7A and B, capacitor C is a frequency compensation capacitor, usually having a value of 10 to 100 pF. This capacitor reduces probability of oscillation. If the voltage on the input marked + is more positive than the voltage on the input marked –, output voltage from the terminal marked + is positive with respect to the center point of + supply and – supply voltages. A negative voltage on + input (in the terms used previously) gives a negative output voltage. The output terminal marked – has opposite polarity to that of the + output terminal. From the aforementioned, it will be seen that a positive voltage on – input will give a negative voltage on + output, and vice versa.



(A)



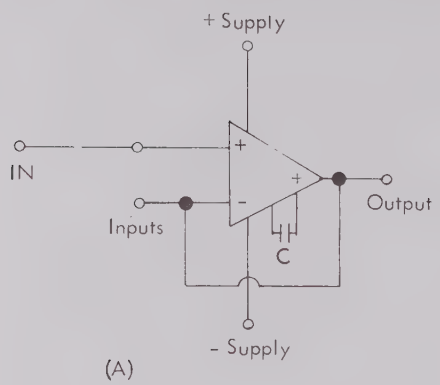
(B)

Figure 7. Operational Amplifiers

22. Operational amplifiers are often used as unity gain amplifiers with very low output impedance. Figure 8A and B show non-inverting and inverting unity gain amplifiers. In Figure 8A, +1 volts above ground (center between + supply and – supply) will drive the output positive. When the output is within a few microvolts of IN, the differential input is only a few microvolts, but this is sufficient to hold the output to +1 volt. The difference between input (IN) and output is approximately IN voltage divided by 100,000 (Gain).

23. In Figure 8B, +1 volts above ground (center between + supply and – supply) will drive the output negative. If the resistance of R1 is exactly equal to the resistance of R2, the potential at the minus input will be zero when output voltage is –1 volts. For output to be –1 volts, – input must be +1 volts divided by 100,000. Output voltage is of opposite polarity to input. The difference between output voltage magnitude and IN voltage magnitude is approximately IN voltage divided by 50,000.

TABLE 3-6. GENERAL CIRCUIT THEORY (CONTINUED)



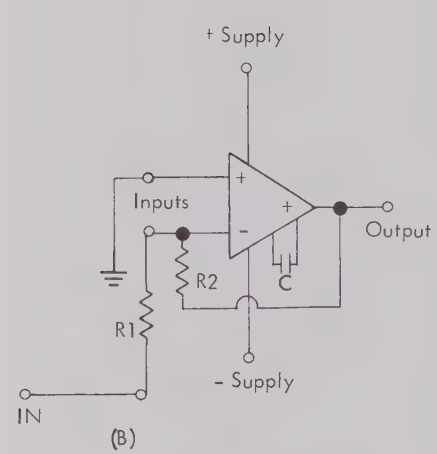


Figure 8. Unity Gain Operational Amplifiers

24. Operational amplifiers are often used as high gain linear amplifiers. In Figure 8B, if the resistance of R2 is 100 times the resistance of R1, the output voltage will be approximately 100 times IN voltage but of opposite polarity. This makes - input zero. For unity gain, here is a drop of one part in 50,000 in the output voltage so that - input voltage will have the valued required to produce the output voltage. This circuit cancels noise due to supply voltage variations; hence it is often used where high fidelity amplification is required.

25. Operational amplifiers are used as integrators. A typical simple circuit is shown in Figure 9. A positive voltage at IN will cause current to flow in R. This raises the voltage at the - input, so the output voltage goes negative, which, via C2, holds the - input voltage at approximately zero. Current through R must, effectively, flow into C2, hence it must also flow out of C2, into the amplifier output. This means that the voltage across C2 increases with time. Since - input voltage is very near ground potential and very near constant, in terms of the voltages usually applied at IN, the current through R is directly proportional to voltage at IN. The voltage across C2 is the exact time integral of the voltage at IN.

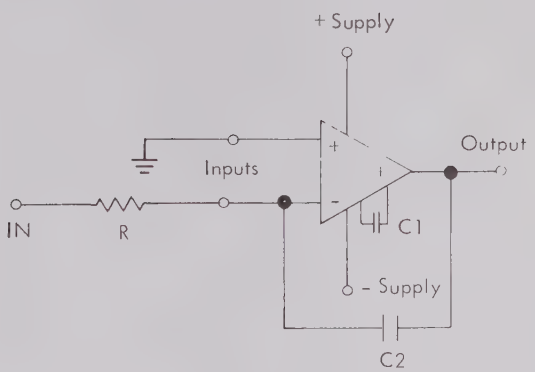


Figure 9. Integrating Operational Amplifiers

26. This circuit is used to produce the integral of a varying voltage, but it is usually used to produce voltage ramps which are linear with time. If the voltage at IN is constant, the output voltage is a linear voltage ramp until a limit of output voltage is reached.

27. Operational amplifiers are used as limit detectors (Figure 10). A differential input of a few microvolts will cause the output voltage of the amplifier to go to one limit. A similar magnitude of differential input, of opposite polarity, will cause the output voltage to go to the opposite limit. If a reference voltage is applied to one input, and an unknown voltage is applied to the other input, the output voltage will show polarity of voltage differences less than 1 millivolt. If the reference is equal to a limit voltage, the output changes polarity as the unknown voltage reaches and passes the limit voltage. This circuit is often used to control linear voltage ramps.

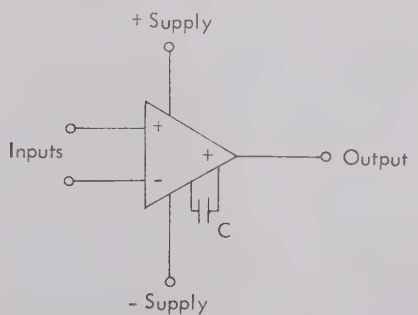


Figure 10. Limit Detector Operational Amplifiers

TABLE 3-6. GENERAL CIRCUIT THEORY (CONTINUED)

28. LOGIC CIRCUITS.

29. The basic logic circuits are AND and OR gates. Symbols are shown in Figure 11. Logic circuits of all kinds usually operate from +5 volt supplies. Power connections are seldom shown in schematic diagrams. Actual signal voltages may vary in magnitude, but the standard signal voltage convention is: Plus 5 Volts is called High (H) or One (1); Zero Volts is called Low (L) or Zero (0). For the symbols shown in Figure 3-14: If both A and B of the AND Gate are 1, output C is 1. If either A or B of the AND Gate is 0, C is 0. If either A or B of the OR Gate is 1, C is 1. If both A and B of the OR Gate are 0, C is 0.

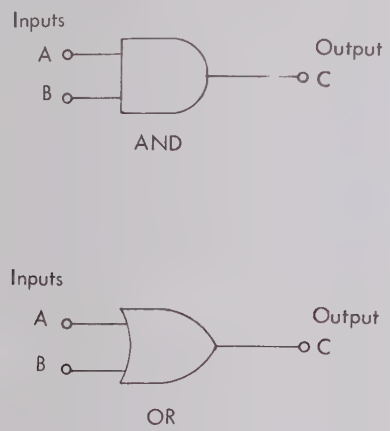


Figure 11. Logic Gate Symbols

30. Figure 12 shows another symbol. A small circle at any signal terminal of a gate reverses the meaning of any signal through the circle. NAND means "Not AND". For A and B both = 1, C is 0 ("Not 1"). NOR means "Not OR". For either A or B = 1, C is 0 ("Not 1"). In the Hybrid OR gate, 0 at A will give 0 at C. 1 at B will give 0 at C. Zero at B and 1 at A will give 1 at C.

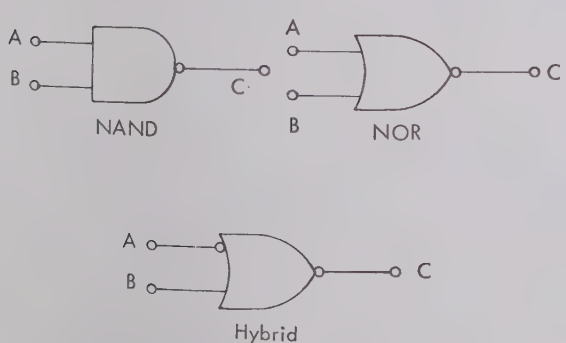


Figure 12. Gate Inversion Symbols

31. Another circuit in common use is the flipflop. This is also called a bistable multivibrator. Figure 13 shows the standard symbol. As with gates, flipflops generally use a +5 volt supply, which is not shown on most schematics.

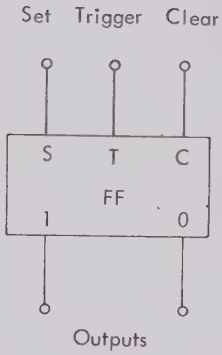


Figure 13. Flipflop

32. The flipflop is a two-state device. If Output 1 is 0, Output 0 is 1. If Output 0 is 0, Output 1 is 1. If there are no signal inputs, the flipflop will maintain its state. A 1 into Set (S) will cause a 1 at Output 1, regardless of past state. A 1 into Clear (C) will cause a 0 at Output 1 (hence a 1 at Output 0) regardless of past state. A 1 pulse into Trigger (T) will reverse the state of the flipflop. The reversal occurs at the leading edge of the pulse. A long pulse (over 5 milliseconds, usually) may cause indeterminate output for some flipflops. Others ignore everything but the positive-going leading edge.

33. Flipflops are used to store logic information in a circuit. This can be contrasted with the immediate transfer of information by amplifiers and by gates.

34. Two circuits of limited use are the other two multivibrators. They are the: (1) free-running MV or oscillator, and (2) monostable MV or one-shot. The free-running MV produces an alternating voltage of approximately square wave form. The one-shot reacts to an incoming 1 pulse by producing a 1 output pulse at a constant time thereafter. Timing of the delay may vary from a fraction of a microsecond to many seconds, or even a few minutes. Usual times are in the millisecond to second range.

TABLE 3-7. TROUBLESHOOTING TRANSISTORS

1. ISOLATING TROUBLE IN TRANSISTOR CIRCUITS.

2. The following procedures and data are given to aid in determining whether a transistor is operational. Tests are given for both in-circuit and out-of-circuit transistors.

3. IN-CIRCUIT TESTING.

4. The common causes of transistor failures are internal short- and open-circuits. In transistor circuit testing the most important consideration is the transistor base-emitter junction. Like the control grid of a vacuum tube, this is the operational control point in the transistor. This junction is essentially a solid state diode. For the transistor to conduct, the diode must conduct; that is, the diode must be forward biased. As with simple diodes, the forward-bias polarity is determined by the materials forming the junction. Use the transistor symbol on the schematic diagram to determine the bias polarity required to forward-bias the base-emitter junction. The A part of Figure 1 shows transistor symbolts with terminals labeled. Notice that the emitter arrow conventionally points toward the type N material. The other two columns of the illustration compare the biasing required to cause conduction and cut-off in transistors and vacuum tubes. If the transistor base-emitter diode (junction) is forward-biased the transistor conducts. If the diode is heavily forward-biased, the transistor saturates. However, if the base-emitter diode is reverse-biased the transistor is cut-off. The voltage drop across a forward-biased emitter-base diode varies with transistor collector current. For example, a germanium transistor has a typical forward-bias, base-emitter voltage of 0.2-0.3 volts when collector current is 10-100 ma. In contrast, forward bias voltage for silicon transistors is about twice that for germanium types: about 0.5-0.6 volts when collector current is low, and about 0.8-0.9 volts when collector current is high.

5. Figure 1, part B, shows simplified versions of the three basic transistor circuits and gives the operating characteristics of each. When examining a transistor stage, first determine if the emitter-base diode is biased for conduction (forward-biased) by measuring the voltage difference between emitter and base. When using an electronic voltmeter, do not measure directly between emitter and base: there may be sufficient loop current between the voltmeter leads to damage the transistor. Instead, measure each voltage separately with respect to a voltage common point (e.g., chassis). If the emitter-base diode is forward-biased, check for amplifier action by short-circuiting base to emitter while observing collector voltage. The short-circuit eliminates base-emitter bias and should cause the transistor to stop conducting (cut off). Collector voltage should then shift to near the supply voltage. Any difference is due to leakage current through the transistor and, in general, the smaller this current, the better the transistor. If collector voltage does not change, the transistor has either an emitter-collector short circuit or emitter-base open circuit.

6. TESTING TRANSISTORS WITH AN OHMMETER.

7. The two common causes of transistor failure are internal short- and open-circuits. Remove the transistor from the circuit and use an ohmmeter to measure internal resistance. See Table 1 for measurement data.

CAUTION

Most ohmmeters can supply enough current or voltage to damage a transistor. Before using an ohmmeter to measure transistor forward or reverse resistance, check open-circuit voltage and short-circuit current output ON THE RANGE TO BE USED. Open-circuit voltage must not exceed 1.5 volts and short-circuit current must be less than 3 ma. See Table 2 for safe resistance ranges for some common ohmmeters.

8. FIELD EFFECT TRANSISTORS (FET)

9. The symbols shown are for simplest construction, non-protected, non-insulated gate FET. Multiple gate and insulated gate FET are also in common use. Operation is similar to operation of vacuum tubes, but both polarities of FET are used. Drain voltages may be in the vacuum tube plate voltage region, but usually are below 50 volts. FET may be saturated or open with zero volts from Gate to source. This depends on construction. Forward voltages on the Gate can seldom cause trouble, but static voltages developed by the technicians clothes may put reverse voltage on the gate sufficient to destroy the FET. For storage and handling the Gate should be shorted to the source. Touch hand, tool, or test probe or clip to the source before touching it to the Gate.

10. To determine whether an FET is in operating condition, leave in the circuit, and apply +1.5V, GND, and -1.5V, in turn, from Gate to Source. Observe change in output voltage. A convenient source of 1.5 volts is your ohmmeter; however an additional meter is required to observe output voltage. DO NOT apply more than 50% of Drain Voltage value as a reverse bias on the Gate. This is a common limit value for noninsulated FET. For non-operating checks of FET, the published static characteristics should be consulted. Variations from one type to another may have ratios of 1,000 or 100,000. Universal tests are not applicable.

TABLE 3-7. TROUBLESHOOTING TRANSISTORS (CONTINUED)

Table 1. Out-of-Circuit Transistor Resistance Measurement

Transistor Type		Connect Ohmmeter: Pos. lead to	Connect Ohmmeter: Neg. lead to	Measure Resistance (ohms) Germanium	Measure Resistance (ohms) Silicon
PNP	Small Signal	emitter	base*	200 - 500	1K - 3K
		emitter	collector	10K - 100 K	very high (might read open)
	Power	emitter	base*	30 - 50	200 - 1000
		emitter	collector	several hundred	high, often greater than 1M
NPN	Small Signal	base	emitter	200 - 500	1K - 3K
		collector	emitter	10K - 100K	very high (might read open)
	Power	base	emitter	30 - 50	200 - 1000
		collector	emitter	several hundred	high, often greater than 1M

* To test for transistor action, add collector-base short. Measured resistance should decrease.

Table 2. Safe Ohmmeter Ranges for Transistor Resistance Measurements

Ohmmeter	Safe Range (s)	Open Ckt Voltage	Short Ckt Current	Lead: Color	Lead: Polarity
H-P 412A	R x 1K	1.0V	1 ma	Red	+
	R x 10K	1.0V	100 µa	Black	-
	R x 100K	1.0V	10 µa		
	R x 1M	1.0V	1 µa		
	R x 10M	1.0V	0.1 µa		
H-P 410C	R x 1K	1.3V	0.57 ma	Red	+
	R x 10K	1.3V	57 µa	Black	-
	R x 100K	1.3V	5.7 µa		
	R x 1M	1.3V	0.5 µa		
	R x 10M	1.3V	0.05 µa		
H-P 410B	R x 100	1.1V	1.1 ma	Black	+
	R x 1K	1.1V	110 µa	Red	-
	R x 10K	1.1V	11 µa		
	R x 100K	1.1V	1.1 µa		
	R x 1M	1.1V	0.11 µa		
Simpson 260	R x 100	1.5V	1 ma	Red	+
				Black	-
Simpson 269	R x 1K	1.5V	0.82 ma	Black	+
				Red	-
Triplett 630	R x 100	1.5V	32 ma	Varies with Serial Number	
	R x 1K	1.5V	3.25 ma		
Triplett 310	R x 10	1.5V	750 µa		
	R x 100	1.5V	75 µa		

TABLE 3-7. TROUBLESHOOTING TRANSISTORS (CONTINUED)

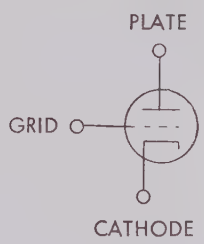
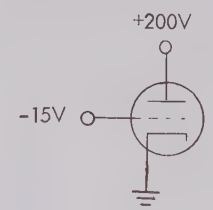
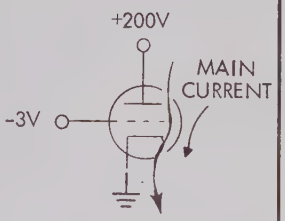
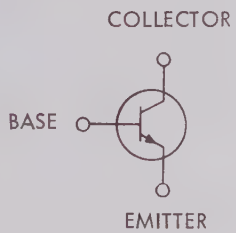
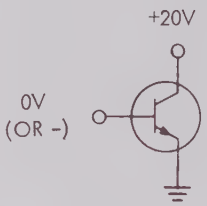
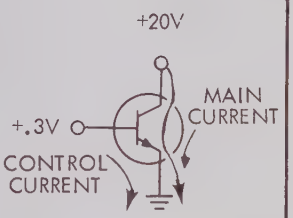
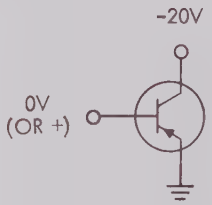
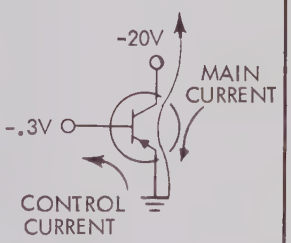
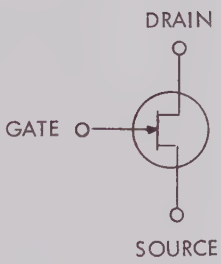
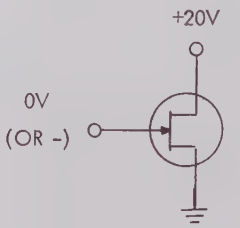
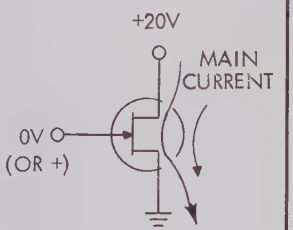
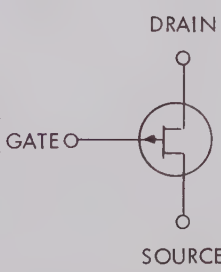
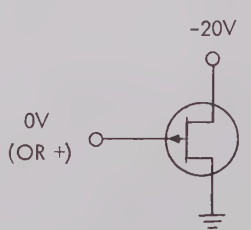
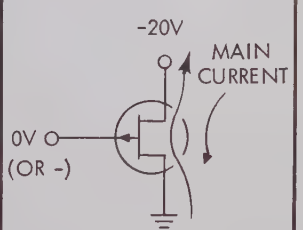
A. TRANSISTOR BIASING			
DEVICE	SYMBOL	CUTOFF	CONDUCTING
VACUUM TUBE			
NPN TRANSISTOR			
PNP TRANSISTOR			
FIELD EFFECT TRANSISTOR N CHANNEL			
FIELD EFFECT TRANSISTOR P CHANNEL			

Figure 1. Transistor Biasing and Operating Characteristics, Page 1 of 2

TABLE 3-7. TROUBLESHOOTING TRANSISTORS (CONTINUED)

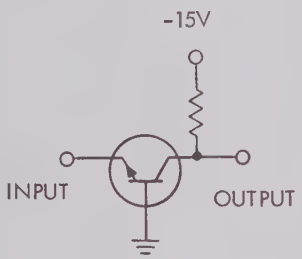
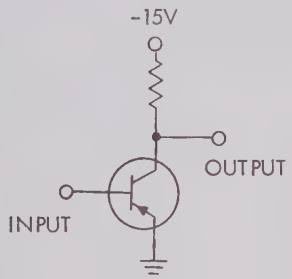
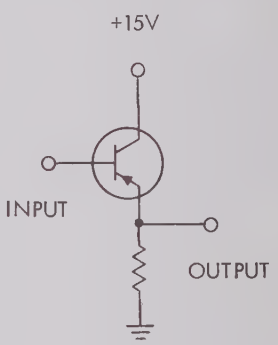
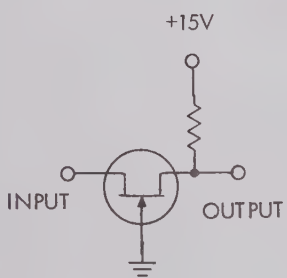
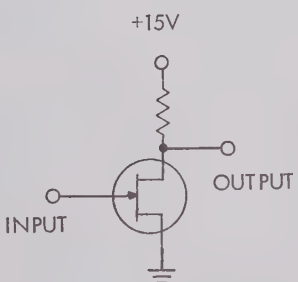
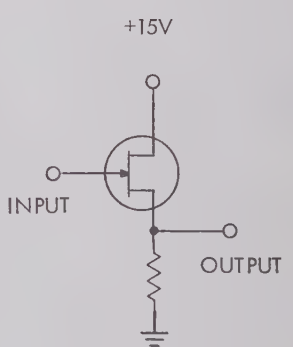
B. AMPLIFIER CHARACTERISTICS			
CHARACTERISTIC	COMMON BASE	COMMON EMITTER	COMMON COLLECTOR
INPUT Z	30-50 Ω	500-1500 Ω	20-500K Ω
OUTPUT Z	300-500K Ω	30-50K Ω	50-1000 Ω
VOLTAGE GAIN	500-1500	300-1000	<1
CURRENT GAIN	<1	25-50	25-50
POWER GAIN	20-30 dB	25-40 dB	10-20 dB
			
INPUT Z	1-200 Ω	100K Ω-10M Ω	100K Ω-10M Ω
OUTPUT Z	10K-500K Ω	10K-500K Ω	1-200 Ω
VOLTAGE GAIN	50-500K	50-2.5K	<1
POWER GAIN	10K-500K	25K-125 x 10^6	100-2 x 10^6
TRANSCONDUCTANCE = 5K to 10^6 μmhos			
			

Figure 1. Transistor Biasing and Operating Characteristics, Page 2 of 2

SECTION IV
MAINTENANCE

4–1. GENERAL.

4-2. This section contains maintenance instructions for the Signal Generator. Included are a list of test equipment required to maintain the instrument, symptomatic and systematic troubleshooting procedures to localize a malfunction to an individual subassembly or circuit, detailed circuit theory, and calibration instructions for restoring the Signal Generator to proper operating condition after the necessary repairs and/or replacements have been effected.

4–3. TEST EQUIPMENT REQUIRED.

4-4. The test equipment required for the maintenance of the Signal Generator is listed in Table 4-1. Instruments of equivalent characteristics may be substituted for any item listed.

TABLE 4-1. TEST EQUIPMENT REQUIRED FOR MAINTENANCE

1.	Digital Voltmeter (AC/DC), Ballantine Model 355
2.	Frequency Counter, Eldorado Electrodata Model 1650
3.	Frequency Counter and Converter, Hewlett-Packard Model 5245L/5253B
4.	Signal Generator, Hewlett-Packard Model 612A
5.	Power Meter, General Microwave Model 454A
6.	Thermistor Mount, General Microwave Model 421C
7.	80 MHz Scope, Tektronix Model 585
8.	Spectrum Analyzer, SINGER Model SA-70
9.	Oscilloscope, Hewlett-Packard Model 130C
10.	Sweep Generator (10 to 550 MHz) Telonic Model 2003
11.	Standing Wave Indicator, Hewlett-Packard Model 415B
12.	RHO-Tector, Telonic Model TRB-3
13.	Standard Mismatch Termination, Telonic Models TRMI-1.20 and TRMI-1.50
14.	50-Ohm Termination, Telonic Type N
15.	Step Attenuator, Kay Model 460A
16.	Pad, 10 dB
17.	Pad (Calibrated), 20 dB
18.	BNC "T", UG-274/U
19.	Type N to BNC Adapter, UG-201A/U
20.	Detector, Hewlett-Packard Model 423A
21.	Pad (Standard), 80 dB
22.	Signal Generator, SINGER Model 6201
23.	Step Attenuator (Standard), 0-70 dB
24.	Test Oscillator, Hewlett-Packard Model 651B
25.	DC Digital Voltmeter, Hewlett-Packard Model 3450A
26.	AC Digital Voltmeter, Fluke 8300A-01
27.	Dual Trace Plug-In, Hewlett-Packard Model 1405A
28.	Pad, 6 dB
29.	Matching Transformer, Applied Research Model 50-93
30.	50-Ohm Series Resistor (1/4 watt metal film resistor mounted in coaxial package containing one male BNC connector and one femal BNC connector)
31.	Subminiature-to-BNC Adapter, Sealectro Model 50-174-6800
32.	Subminiature Plug, Sealectro Model 51-007-0000
33.	Subminiature Jack, Sealectro Model 51-008-0000

4–5. TROUBLESHOOTING.

4-6. COMPONENT LOCATIONS.

4-7. The locations of the major assemblies and test points are illustrated in Figure 4-1. To gain access to these components, remove the top cover plate as directed in the following steps.

a. With the Signal Generator withdrawn from line power, loosen and remove the single screw (located at the center of the rear panel top lip) that secures the position of the top cover plate.

b. Grasp the cover plate and slide it to the rear of the Signal Generator until it is completely disengaged.

4-8. POWER SUPPLY CHECKS.

4-9. Improper operation of the Signal Generator may be due to a malfunction within power supply assembly A9 or one or more of the regulators within this circuitry delivering out-of-limit voltages. To ascertain that the individual power supplies are operating properly, or to localize a malfunction, proceed as directed in Table 4-2.

NOTE

The -26 volt supply serves as the reference for the +12, +5 and -5.2 volt supplies; and the +12 volt supply serves as a reference for the +6 volt supply. In addition, the +12 and -26 volt supplies provide +V and -V supplies, respectively, to the IC difference amplifiers in the +12, +6, +5 and -5.2 volt supplies. Consequently, if the -26 volt supply must be adjusted to obtain the proper output level, it will be necessary to check the output levels of the +12, +6, +5 and -5.2 volt supplies. Similarly, if the +12 volt supply output is adjusted, it will be necessary to check the output levels of the +6, +5 and -5.2 volt supplies.

TABLE 4-2. POWER SUPPLY CHECKOUT PROCEDURE

Step	Procedure	Normal Indication
1	Check the output of the -26 volt supply by connecting the "high" lead of a Ballantine 355 Digital Voltmeter (set to the -100 VDC range) to any one of the "-26V ORN" terminals of TB2; connect the "common" lead to any of the "GRD BLK" terminals of TB2. Connect the vertical input terminals of an H-P 130C oscilloscope (AC-coupled) to the same terminals as the voltmeter. Note both the voltmeter indication and the oscilloscope display.	Voltmeter indicates between -25.50 and -26.50 volts; ripple is 1 millivolt peak-to-peak or less. Adjust A9A2R7 (Figure 4-2) is required.
2	Check the output of the +12 volt supply by connecting the "high" lead of the Ballantine 355 Voltmeter (set to the +100 VDC range) to any one of the "+12V RED" terminals of TB2; connect the "common" lead to any one of the "GRD BLK" terminals of TB2. Connect the vertical input terminals of the oscilloscope (AC-coupled) to the same terminals as the voltmeter. Note both the voltmeter indication and the oscilloscope display.	Voltmeter indicates between +11.50 and +12.50 volts; ripple is 2 millivolts peak-to-peak or less. Adjust A9A2R17 (Figure 4-2) if required.
3	Check the output of the -5.2 volt supply connecting the "high" lead of the Ballantine 355 Voltmeter (set to the -10 VDC range) to any one of the "-5.2V GRN; terminals of TB2; connect the "common" lead to any of the "GRD BLK" terminals of TB2. Connect the vertical input terminals of the oscilloscope (AC-coupled) to the same terminals as the voltmeter. Note both the voltmeter indication and the oscilloscope display.	Voltmeter indicates between -5.15 and -5.25 volts; ripple is 2 millivolts peak-to-peak or less. Adjust A9A2R23 (Figure 4-2) if required.
4	Check the output of the +5 volt supply by connecting the "high" lead of the Ballantine 355 Voltmeter (set to the +10 VDC range) to any one of the "+5V YEL" terminals of TB2; connect the "common" lead to any one of the "GRD BLK" terminals of TB2. Connect the vertical input terminals of the oscilloscope (AC-coupled) to the same terminals as the voltmeter. Note both the voltmeter indication and oscilloscope display.	Voltmeter indicates between +4.95 and +5.05 volts; ripple is 2 millivolts peak-to-peak or less. Adjust A9A2R29 (Figure 4-2) if required.
5	Check the output of the +6 volt supply by connecting the lead of the Ballantine 355 Voltmeter (set to the +10 VDC range) to any one of the "+6V BLU" terminals of TB2; connect the "common" lead to any one of the "GRD BLK" terminals of TB2. Connect the vertical input terminals of the oscilloscope (AC-coupled) to the same terminals as the voltmeter. Note both the voltmeter indication and oscilloscope display.	Voltmeter indicates between +5.95 and +6.05 volts; ripple is 10 millivolts peak-to-peak or less. Adjust A9A2R35 (Figure 4-2) if required.

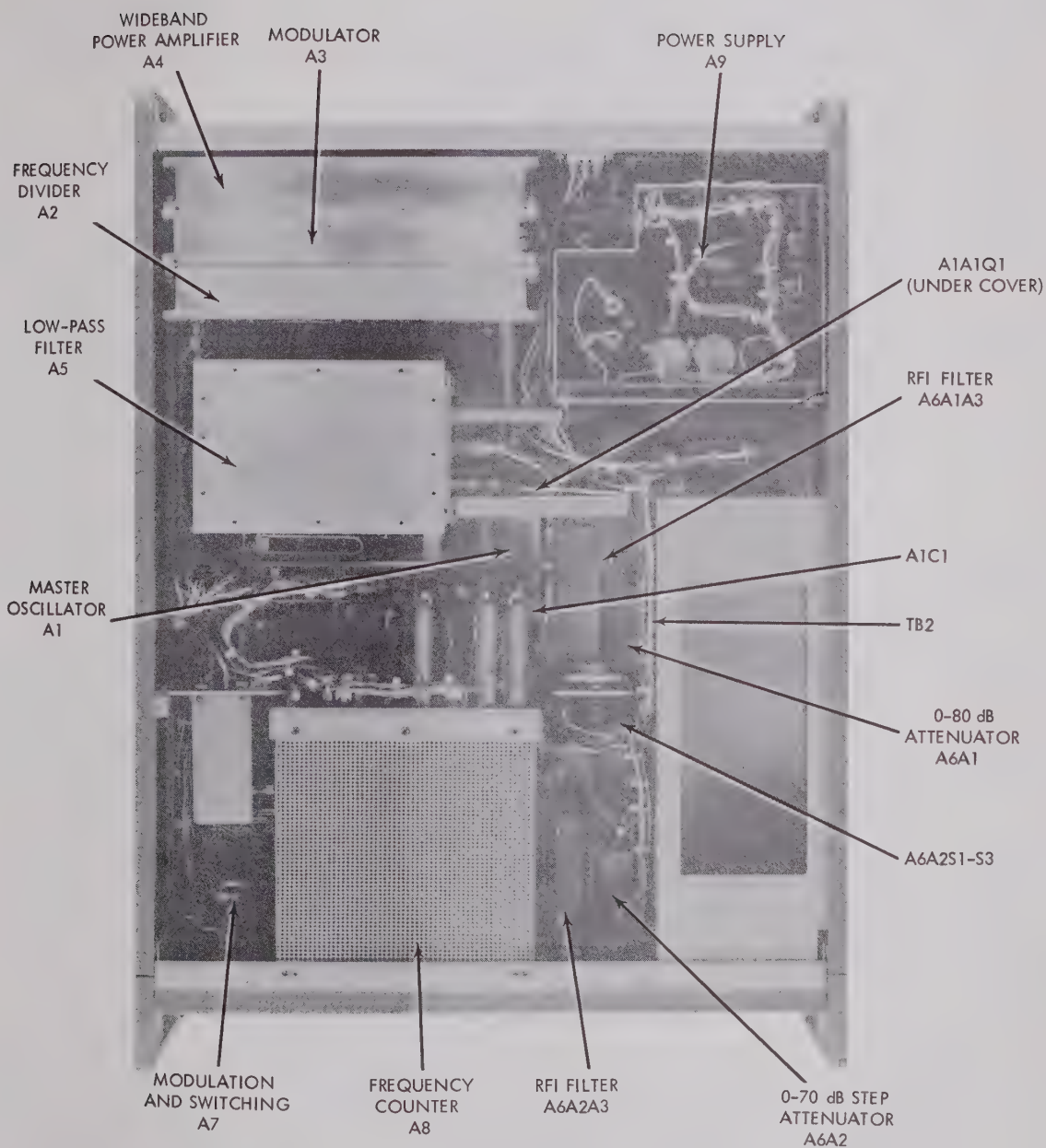


Figure 4-1. Top View of Signal Generator (Cover Removed)

4-10. TROUBLE LOCALIZATION.

4-11. The selectable frequency bands, modulation modes and frequency counter modes enable the technician to isolate a malfunction to a group of circuits by symptomatic troubleshooting procedures. Once the malfunction has been isolated to a particular circuit grouping, systematic trouble localization procedures will lead the technician to the defective component. Table 4-3 is a symptomatic troubleshooting guide which references the technician to the proper checkout, replacement and/or calibration procedure necessary to restore the Signal Generator to normal operating condition.

4-12. CHECKOUT PROCEDURES.

4-13. Paragraphs 4-14. through 4-47. detail the test procedures to be employed to determine whether an individual assembly within the Signal Generator is operating properly.

TABLE 4-3. SYMPTOMATIC TROUBLE LOCALIZATION GUIDE

Symptom	Possible Cause and Checkout Procedure	Assembly No.	Paragraph
No RF output for any setting of the RANGE MHz and dBm switches; frequency counter functions only in external count operation.	1. Master oscillator inoperative.	A1	4-14.
	2. Frequency divider inoperative	A2	4-19.
	3. Modulator inoperative.	A3	4-23.
No RF output for any setting of the RANGE MHz and dBm switches; frequency counter functions normally.	1. Modulator inoperative.	A3	4-23.
	2. Wideband power amplifier inoperative.	A4	4-26.
	3. Low-pass filter inoperative.	A5	4-31.
	4. Output attenuator inoperative.	A6	4-36.
	5. Modulation and switching inoperative.	A7	4-40.
No RF output for one or more (but not all) settings of the RANGE MHz switch; frequency counter may or may not function normally.	1. Frequency divider inoperative.	A2	4-19.
Excessive harmonic content in RF output; loss of RF power at upper half of any band.	1. Oscillator board inoperative.	A8A3A6	4-42.
	2. Low-pass filter inoperative.	A5	4-31.
No AM modulation	1. Modulator inoperative.	A3	4-23.
	2. Modulation and switching inoperative.	A7	4-40.
Excessive FM on AM	1. Master oscillator defective.	A1	4-14.
	2. Power supply defective.	A9	4-8.
1 kHz internal modulation inoperative	1. Modulation and switching inoperative.	A7	4-40.
No FM modulation	1. Modulation and switching inoperative.	A7	4-40.
Frequency lock mode inoperative	1. Low-pass filter inoperative.	A5	4-31.
	2. AFC board inoperative.	A8A3A7	4-42.
No pulse modulation	1. Modulator inoperative	A3	4-23.
	2. Modulation and switching inoperative.	A7	4-40.
Frequency counter inoperative on one band only	1. Low-pass filter inoperative	A5	4-31.

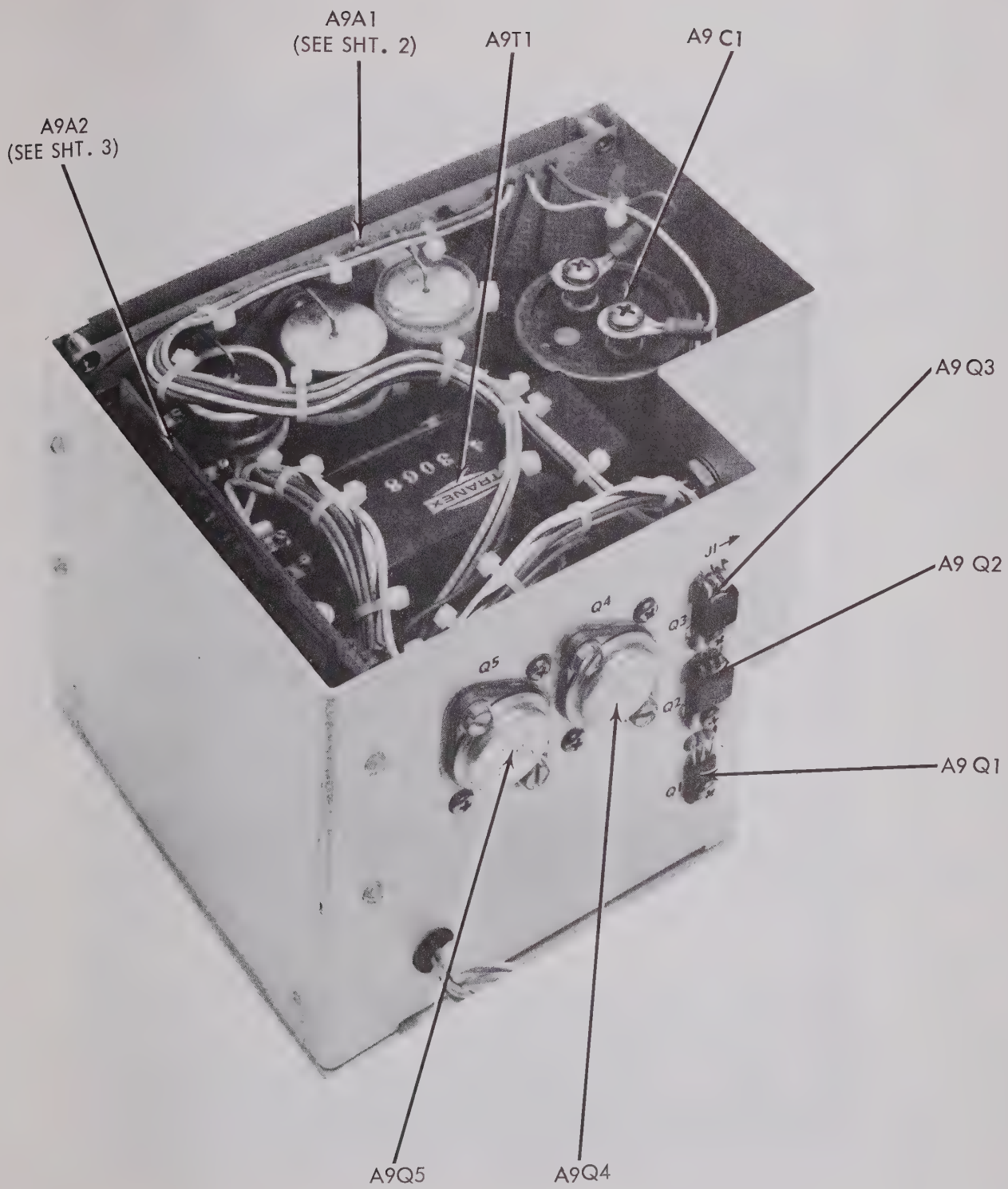


Figure 4-2. Power Supply **A9** (Sheet 1 of 3)

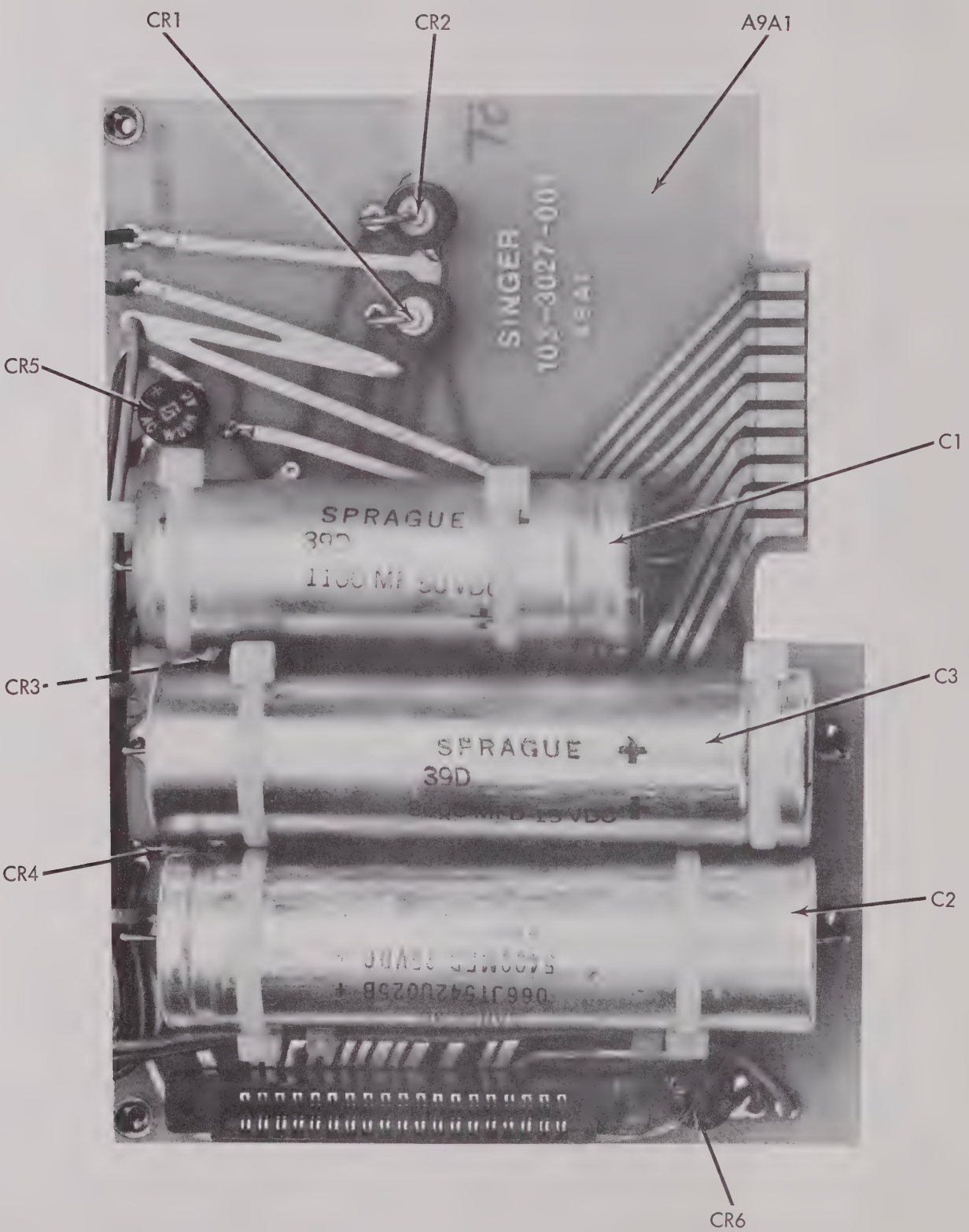


Figure 4-2. Power Supply **A9** (Sheet 2 of 3)

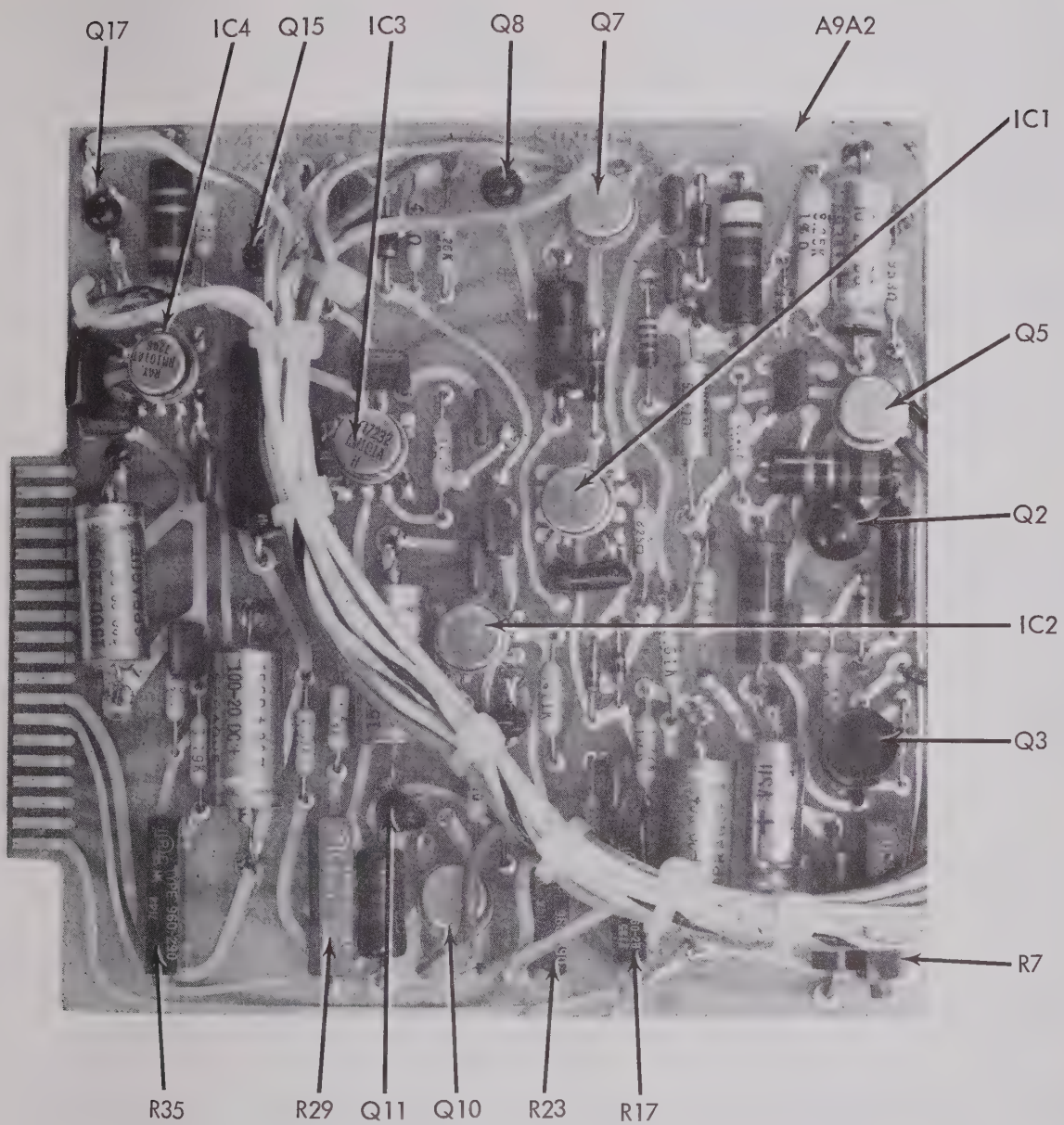


Figure 4-2. Power Supply **A9** (Sheet 3 of 3)

4-14. MASTER OSCILLATOR A1

4-15. Prior to performing the checks of paragraphs 4-16 through 4-18, check that the proper operating voltages are being applied to A1 (refer to Table 4-4).

4-16. Frequency Range.

a. Set the VERNIER frequency control to mid-range and with the CW pushbutton pressed, disconnect A2J1 from A1J1. Couple A1J1 to an H-P 5245L/5253B electronic counter/frequency converter through a 10 dB, 50 ohm pad.

b. Rotate the FREQUENCY control fully clockwise and determine the master oscillator output frequency; it should be at least 512 MHz. Rotate the FREQUENCY control fully counterclockwise and again determine the output frequency; it should be below 248 MHz. If both of these frequency indications are obtained, proceed to paragraph 4-17. Ohterwise, it may be necessary to reset the stop gear to be sure of a tuning range from 248 to 512 MHz.

CAUTION

Do not tune the oscillator above 525 MHz during the adjustment process; damage may result. (Typical OSC range from 520-246.)

4-17. Output Level.

a. With the VERNIER frequency control set to mid-range, the CW pushbutton is pressed, the FREQUENCY control rotated fully counterclockwise and A2P1 disconnected from A1J1, couple an H-P 478A/431C thermistor mount/power meter to A1J1 via a 10 dB, 50 ohm pad.

b. Note the power meter indication; it should read a minimum of -7 dBm (corresponding to a master oscillator output level of +3 dBm).

c. While continuously monitoring the power meter indication, slowly rotate the FREQUENCY control clockwise, until the high end stop is reached; the power meter should read at least -7 dBm throughout the band. If the output power requirements are obtained, proceed to paragraph 4-18.

4-18. Spurious Outputs.

a. Tune a Singer Model SA-70 Wide Dispersion Microwave Spectrum Analyzer to 500 MHz, a dispersion of 130 MHz/division, a bandwidth of 200 kHz, a sweep time of 3 msec/division and a logarithmic amplitude display. With no signal coupled to the analyzer, adjust the IF gain for a noise display one division high and set the RF attenuator for 30 dB insertion.

TABLE 4-4. ASSEMBLY POWER DISTRIBUTION

Assembly	Voltage	Point of Application
Master Oscillator A1	-26 volts -26 volt return (ground)	A1C1 (violet lead of orange/black twisted pair from TB2). Ground lug on A1C1 (black lead of orange/black twisted pair from TB2).
Frequency Divider A2	+12 volts -5.2 volts	A2FL1C2 (red lead of red/green twisted pair from A3). A2FL1C1 (green lead of red/green twisted pair from A3).
Modulator A3	+12 volts -5.2 volts	A3A4C1 (red lead from TB2). A3A4C2 (green lead from TB2).
Wideband Power Amplifier A4	+12 volts -5.2 volts	Junction of A4A1C67 and A4A1L37 (red lead from A3A5C1). Junction of A4A1C69 and A4A1L40 (green lead from A3A5C2).
Low Pass Filter A5	+6 volts +5 volts -26 volts Ground	A5A1A5C1 (blue lead from TB2). A5A3J1-19 & -W (yellow lead from TB2) via P1-19 & -W. A5A3J1-3 (orange lead from TB2) via P1-3. A5A3J1-1 & -A (black lead from TB2) via P1-1 & -A.
Output Attenuator A6	+6 volts Ground	A6A1A3C1 and A6A2A3C1 (blue lead from TB2). Ground lug on A6 (black lead from TB2).
Modulation and Switching A7	+12 volts -26 volts -5.2 volts Ground	A7J1-V (red lead from TB2) via P2-V. A7J1-12 (orange lead from TB2) via P2-12. A7J1-U (green lead from TB2) via P2-U. A7J1-D & -F (black lead from TB2) via P2-D & -F.
Frequency Counter A8	+5 volts -26 volts Ground	A8P2-10 & -L (blue lead via A5A3J2-10 & -L. A8P2-C (violet lead) via A5A3J2-C. A8P2-1 & -A (black lead) via A5A3J2-1 & -A.

b. With the VERNIER control set to mid-range, the CW pushbutton pressed and the FREQUENCY control set fully clockwise, couple A1J1 to the spectrum analyzer. Adjust the analyzer RF and/or IF attenuators to obtain a convenient display.

c. While continuously monitoring the spectrum analyzer display, slowly rotate the FREQUENCY control counterclockwise until the low frequency stop is reached. The master oscillator output should be continuous (i.e., no tearing or breaking-up).

4-19. FREQUENCY DIVIDER **A2**

4-20. To check assembly A2 for proper operation, first separate it from assembly A3 as directed in steps a through d of paragraph 4-147, temporarily replace assembly A2 into the Signal Generator as directed below and then perform the checks of paragraphs 4-21 and 4-22.

a. With the RANGE MHz switch set to 62-128, carefully place A2 into the Signal Generator so that the pin on the lever arm of A2A1S1 mates with the slot of the lever arm on the RANGE MHz switch shaft. Position A2 so that its two threaded mounting holes are directly above their mating holes on the main chassis bottom plate. Secure A2 to the bottom plate using two of the screws removed in step b of paragraph 4-147.

b. Check that the proper operating voltages are being applied to A2 (refer to Table 4-4).

4-21. Output Waveforms.

a. Set the RANGE switch to 248-512 and rotate the FREQUENCY control fully counterclockwise.

b. Couple A2P1 to A1J1. Insert the tip of an oscilloscope probe into the center conductor of A2J1; connect the probe ground lead to A2 ground. Couple the probe to the input of a Tektronix 561B sampling oscilloscope.

c. Observe the oscilloscope display; a waveform similar to that illustrated in Figure 4-3 should appear. Slowly rotate the FREQUENCY control throughout its tuning range, while monitoring the display; the display should be similar to Figure 4-3 at all frequencies within the band.

d. Repeat step c with the RANGE MHz switch set, in sequence, to 124-256, 62-128, 31-64, 15.5-32 and 7.75-16.

e. Disconnect W2P1 from A2J2 and couple the sampling scope to A2J2. Repeat step c.

f. Disconnect P6 from A2J3 and couple the sampling scope to A2J3. Repeat step c.

g. If the required output waveforms are obtained, proceed to paragraph 4-22; if they are not, remove the shield plate from A2 (refer to paragraph 4-147e) and effect the necessary repairs and/or replacements (refer to Table 4-12 and see Figure 4-4).

4-22. Output Power.

a. Couple A2J1 to an H-P 478A/431C thermistor mount/power meter through a 6 dB pad. Set the RANGE MHz switch to 248-512 and slowly rotate the FREQUENCY control throughout its range while noting the power meter reading; the power meter should indicate at least -36 dBm (corresponding to a minimum frequency divider output level of -30 dBm) throughout the band. Repeat the above for RANGE MHz switch settings of 124-356, 62-128, 31-64, 15.5-32 and 7.75-16.

b. Connect a Tektronix 585 oscilloscope to A2J2 and again rotate the FREQUENCY control throughout its range; the peak-to-peak indication should be at least 2.0 volts.

c. Connect the oscilloscope to A2J3 and again rotate the FREQUENCY control throught its range; the peak-to-peak indication should be at least 0.65 volt.

4-23. MODULATOR **A3**

4-24. To check assembly A3 for proper operation, first separate it from assembly A4 (refer to steps a and b of paragraph 4-148) and then replace both A2 and A3 back into the main chassis (refer to step a of paragraph 4-20). Check that the required operating voltages are being applied (refer to Table 4-4).

a. Set the front panel controls as indicated below.

Control	Setting
RANGE MHz switch	248 - 512
FREQUENCY control	Mid-range
CW pushbutton	Pressed
dBm continuous control	Fully clockwise
VX2 pushbutton	Released
AM/FM switch	AM

b. Connect A2P1 to A1J1 and couple A3A2P2 to an H-P 478A/431C thermistor mount/power meter. Note the power meter indication; it should read at least -18 dBm.

c. Set the RANGE MHz switch, in sequence, to 124-256, 62-128, 31-64, 15.5-32 and 7.75-16 and for each setting, note the power meter indication; it should be at least -25 dBm.

d. Disconnect the thermistor mount/power meter from A3A2P2. Tune a Singer Model SA-70 Wide Dispersion Microwave Spectrum Analyzer to 600 MHz, set for a dispersion of 300 Hz/division, a bandwidth of 200 kHz, a sweep speed of 3 msec/division and a logarithmic amplitude display. Set the RF input attenuator for 30 dB insertion and adjust the IF gain control to obtain a noise display one division high.

e. Couple the spectrum analyzer to A3A2P2 and adjust the FREQUENCY control to center the signal pip on the analyzer display. Adjust the analyzer RF and IF attenuators to obtain a full-scale display.

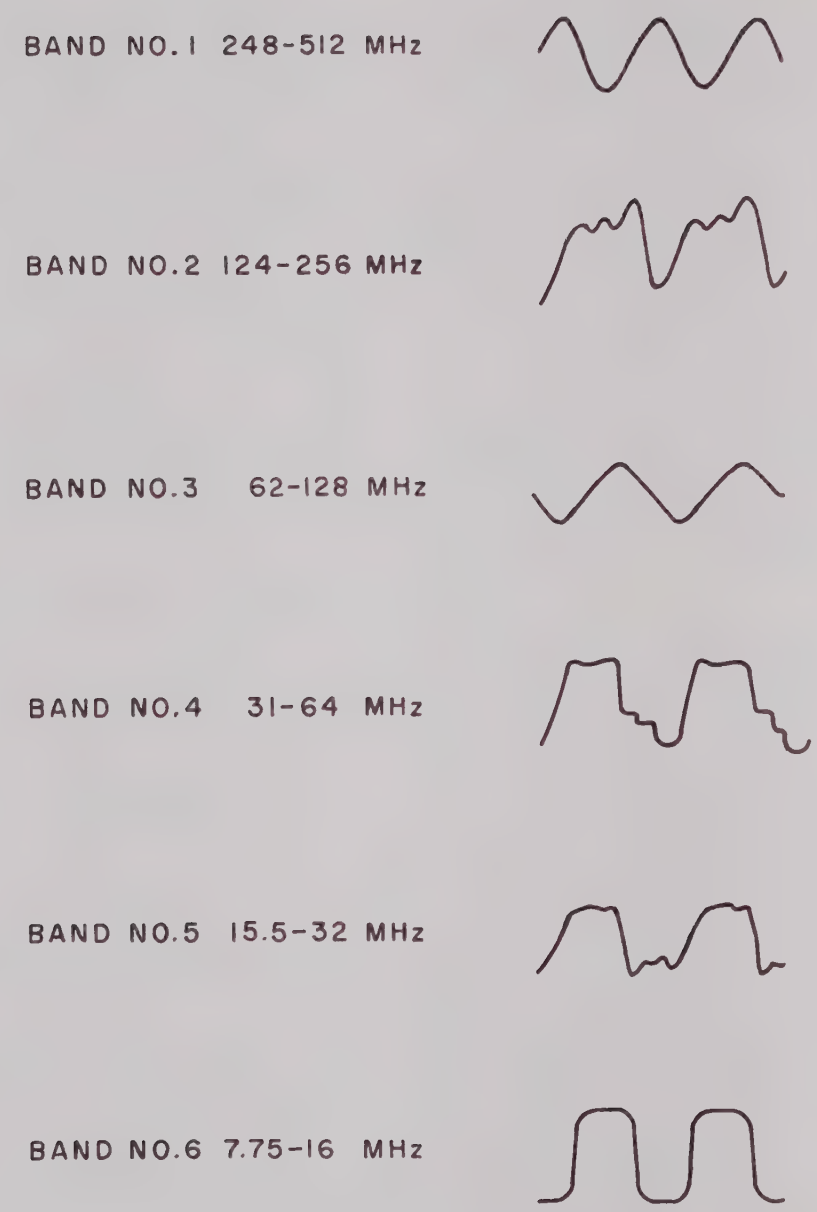


Figure 4-3. Typical Frequency Divider Output Waveforms

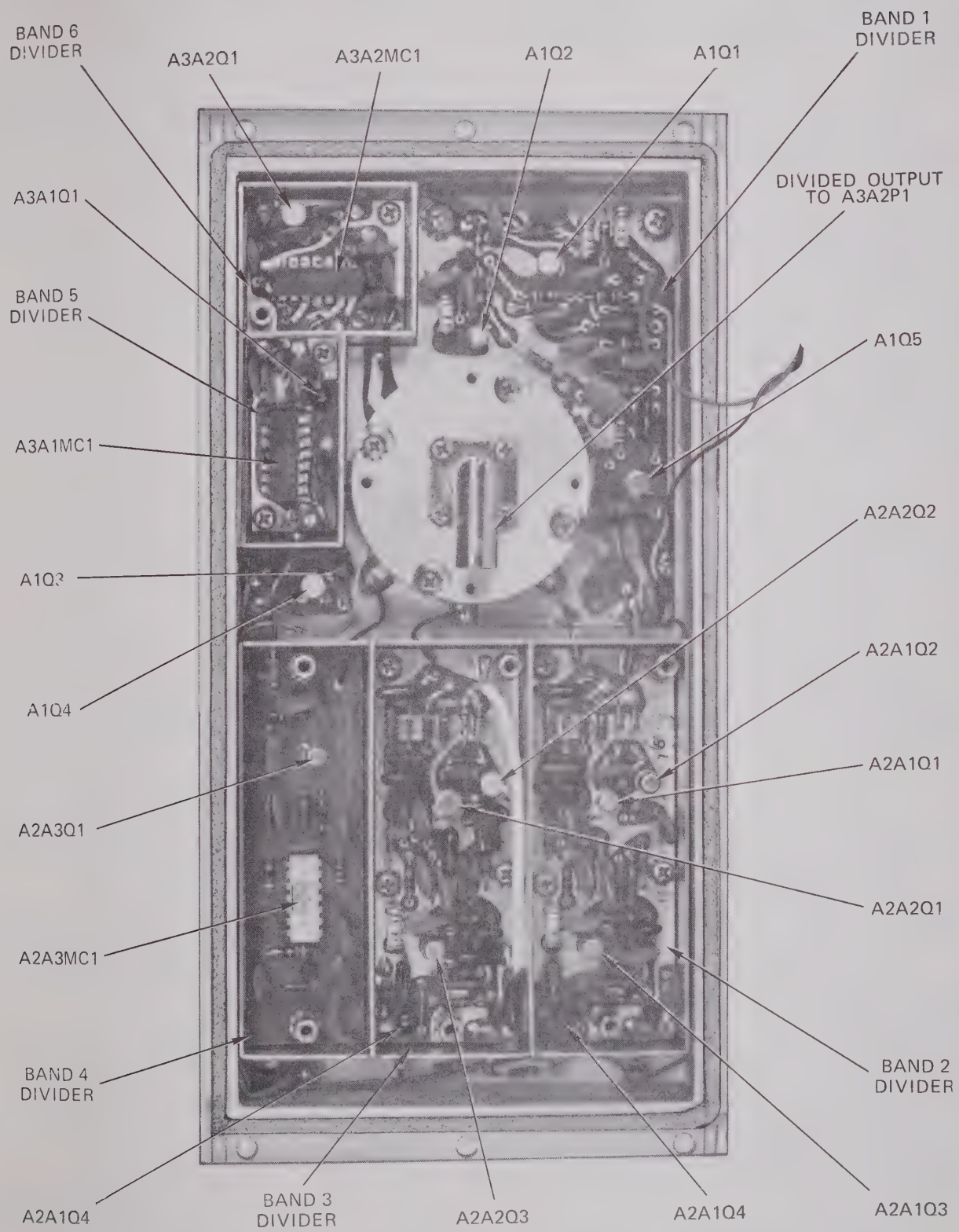


Figure 4-4. Frequency Divider Assembly **A2**

f. Press the AM INT pushbutton. Adjust the AM LEVEL control to obtain an indication of 100 on the % AM meter. Observe the spectrum analyzer display. The full-scale centered signal pip and two signal pips (each typically 3.5 cm from center) which are 6 dB below full scale should be observed on the spectrum analyzer display.

g. With no signal coupled to the AM/PULSE connector, press the AM PULSE pushbutton and note the display response; the centered signal pip should decrease typically 50 dB from full scale.

4-25. If the indications of paragraph 4-24 were obtained, the modulator is operating properly. If these results were not obtained, check A3 for typical voltage levels (refer to Table 4-13 and see Figure 4-5).

4-26. WIDEBAND POWER AMPLIFIER **A4**

4-27. To check A4 for proper operation, first separate it from A3 (refer to steps a through c of paragraph 4-149) and then replace both A2 and A3 back into the main chassis (refer to step a of paragraph 4-20). Check that the required operating voltages are being applied (refer to Table 4-4).

4-28. Gain.

a. Adjust a Telonic 2003 sweep signal generator for a leveled swept output from 10 to 520 MHz and set the RF attenuators and vernier control for minimum output level.

b. Interconnect the equipment as illustrated in Figure 4-6A.

c. Adjust the sweep generator RF attenuators to obtain an oscilloscope display having a maximum amplitude of 6 cm. Using a china marker, trace the response on the oscilloscope graticule. Note and record the total attenuation inserted on the sweep generator.

NOTE

Do not reset the sweep generator vernier control until specifically directed.

d. Reset the sweep generator output attenuator for minimum output level and reconnect the equipment as illustrated in Figure 4-6B.

e. Adjust the sweep generator output attenuator until the highest point of the display coincides with the line drawn in step c. Note the total attenuation inserted on the sweep generator and subtract the value of attenuation recorded in step c from this; the difference should be typically 50 dB.

f. Adjust the sweep generator output attenuator until the lowest point of the display coincides with the line drawn in step c. Note the total attenuation inserted by the sweep generator and subtract the value of attenuation recorded in step c from this; the difference should be typically 39 dB.

4-29. Power Output.

a. Adjust a Telonic 2003 sweep signal generator for a leveled RF output at 10 MHz and adjust its output attenuators for minimum output level. Couple the sweep generator output directly to an H-P 478A/431C thermistor mount/power meter and adjust the sweep generator output level to obtain a power meter indication of -15 dBm.

b. Interconnect the equipment as illustrated in Figure 4-6C. Note the power meter reading; it should be in excess of +2 dBm (corresponding to a wide band power amplifier output level in excess of 125 milliwatts). Tune the sweep generator from 10 to 520 MHz while continuously monitoring the power meter; the power meter should read at least 125 mW (+1 dBm) across the 10 to 520 MHz range.

NOTE

If, at frequencies above 100 MHz, the power meter reading drops below 125 mW, it may be due to overdriving A4. Reduce the sweep generator output level slightly and repeat the procedure. The minimum output power level of A4 should be in excess of 125 mW from 10 to 520 MHz range.

4-30. A malfunction within the wideband power amplifier (see Figure 4-7) can be localized using signal tracing techniques in conjunction with the voltage measurements furnished in Table 4-14.

4-31. LOW-PASS FILTER **A5**

4-32. Prior to checking the low-pass filter assembly, ascertain that the proper operating voltages are being applied to assembly A5 (refer to Table 4-4).

4-33. Frequency Response.

a. Disconnect A4P1 from A5A1J1 and disconnect A5A1P1 from A6A1AT1J1.

b. Set the RANGE MHz switch to 248-512 and rotate the FREQUENCY control fully clockwise.

c. Tune a signal generator (refer to Table 4-5) to a reference frequency of 360 MHz, at an output level of 0 dBm.

d. Interconnect a series 50 ohm calibrating resistor in the test setup of Figure 4-8, and adjust signal generator RF output level to set a reference on the power meter.

e. Connect the low-pass filter in place of the 50 ohm series resistor and note the power meter reading; the change from the reference is the insertion loss of the low-pass filter at the reference frequency and should be typically 1 dB (refer to Table 4-5).

f. Increase the signal generator frequency and note the frequencies at which the specified responses of Table 4-5 occur.

g. Repeat steps b through f for all other settings of the RANGE MHz switch and FREQUENCY control listed in Table 4-5.

h. A malfunction within the low-pass filter (see Figure 4-9) can be localized using voltage measurements in Table 4-15.

TABLE 4-5. LOW-PASS FILTER RESPONSE CHARACTERISTICS

RANGE MHz Switch Setting	RANGE MHz Control Setting	Reference Frequency	Typical Insertion Loss (at f ref)	Typical Frequency Response [1,2]		
				Flatness	-3 dB	-31.5 dB
248-512	Fully cw	360 MHz	0.5 dB	±0.5 dB to 512 MHz	532 MHz	716 MHz
248-512	Fully ccw	256 MHz	0.5 dB	±0.5 dB to 358 MHz	372 MHz	500 MHz
124-256	Fully cw	177 MHz	0.5 dB	±0.5 dB to 265 MHz	266 MHz	358 MHz
124-256	Fully ccw	125 MHz	0.5 dB	±0.5 dB to 179 MHz	186 MHz	250 MHz
62-128	Fully cw	89.5 MHz	1 dB	±1 dB to 128 MHz	133 MHz	179 MHz
62-128	Fully ccw	60 MHz	1 dB	±1 dB to 89.5 MHz	93 MHz	125 MHz
31-64	Fully cw	44 MHz	1 dB	±1 dB to 64 MHz	66.5 MHz	89.6 MHz
31-64	Fully ccw	31 MHz	1 dB	±1 dB to 44 MHz	46.5 MHz	62.5 MHz
15.5-32	Fully cw	22 MHz	1 dB	±1 dB to 32 MHz	33.3 MHz	44.8 MHz
15.5-32	Fully ccw	15 MHz	1 dB	±1 dB to 22.4 MHz	23.2 MHz	31.25 MHz
7.75-16	Fully cw	11 MHz	1 dB	±1 dB to 16 MHz	16.6 MHz	22.4 MHz
7.75-16	Fully ccw	7.75 MHz	1 dB	±1 dB to 11.2 MHz	11.6 MHz	15.62 MHz

1. With respect to reference frequency.

2. Use an H-P 612A signal generator for frequencies above 500 MHz; use a 6201 for frequencies below 500 MHz.

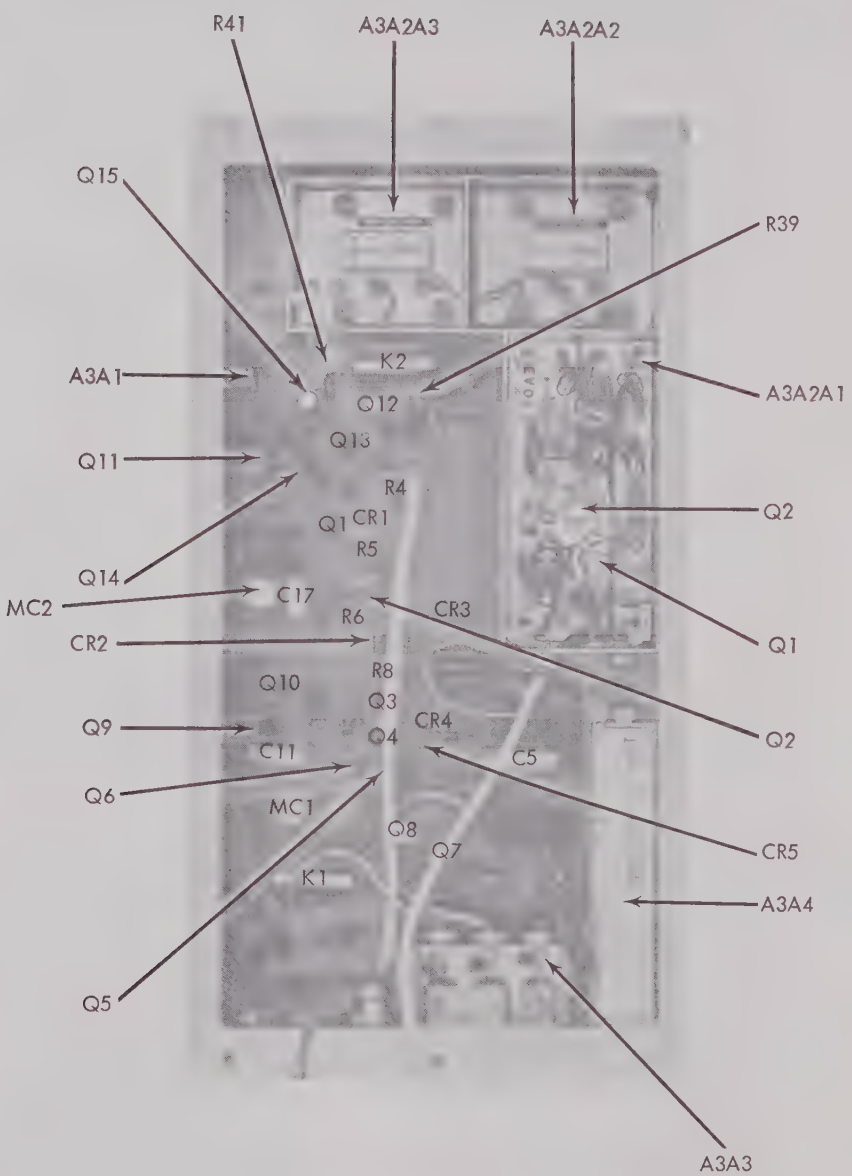


Figure 4-5. Modulator Assembly **A3**

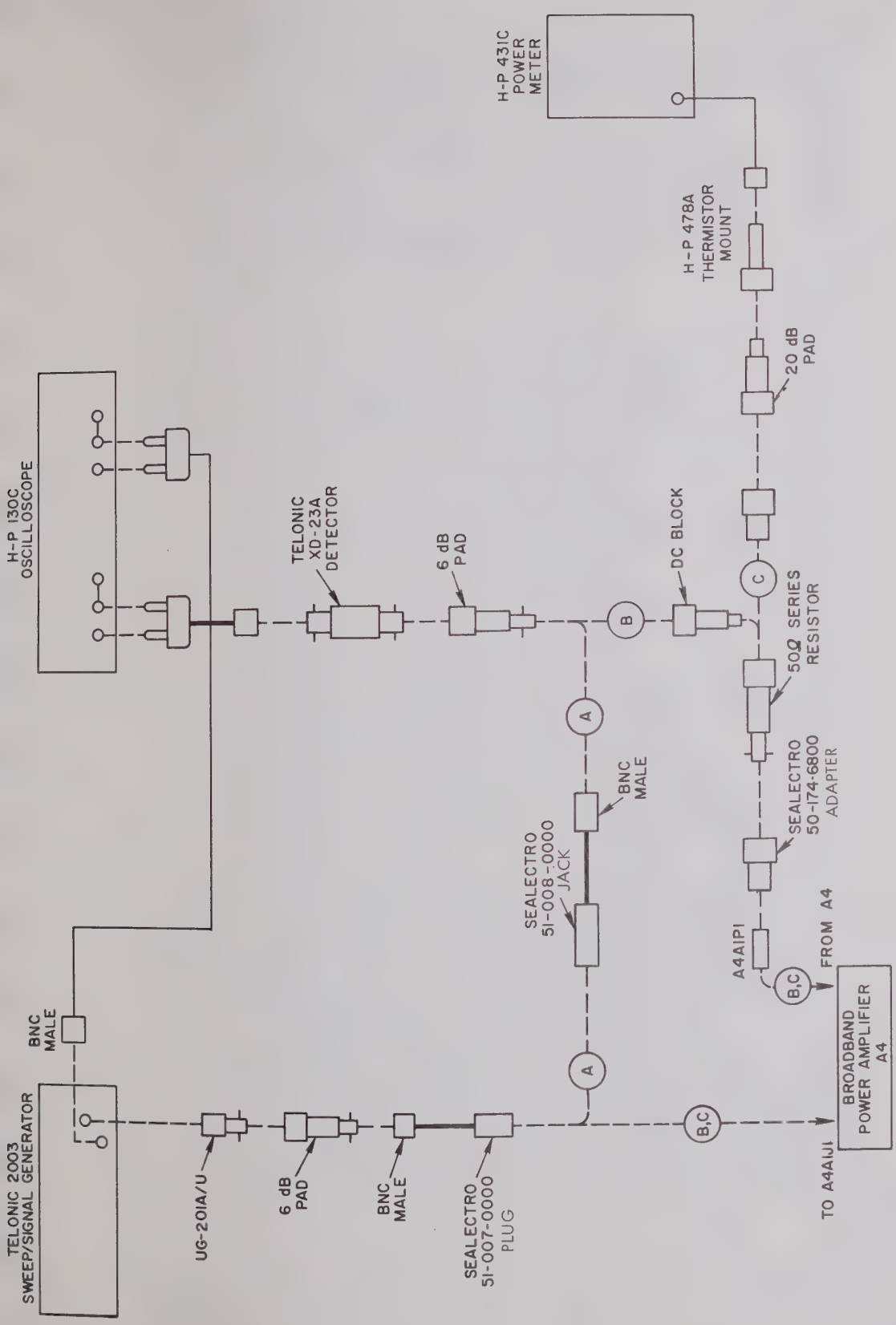


Figure 4-6. Equipment Setup for Wideband Power Amplifier Checkout

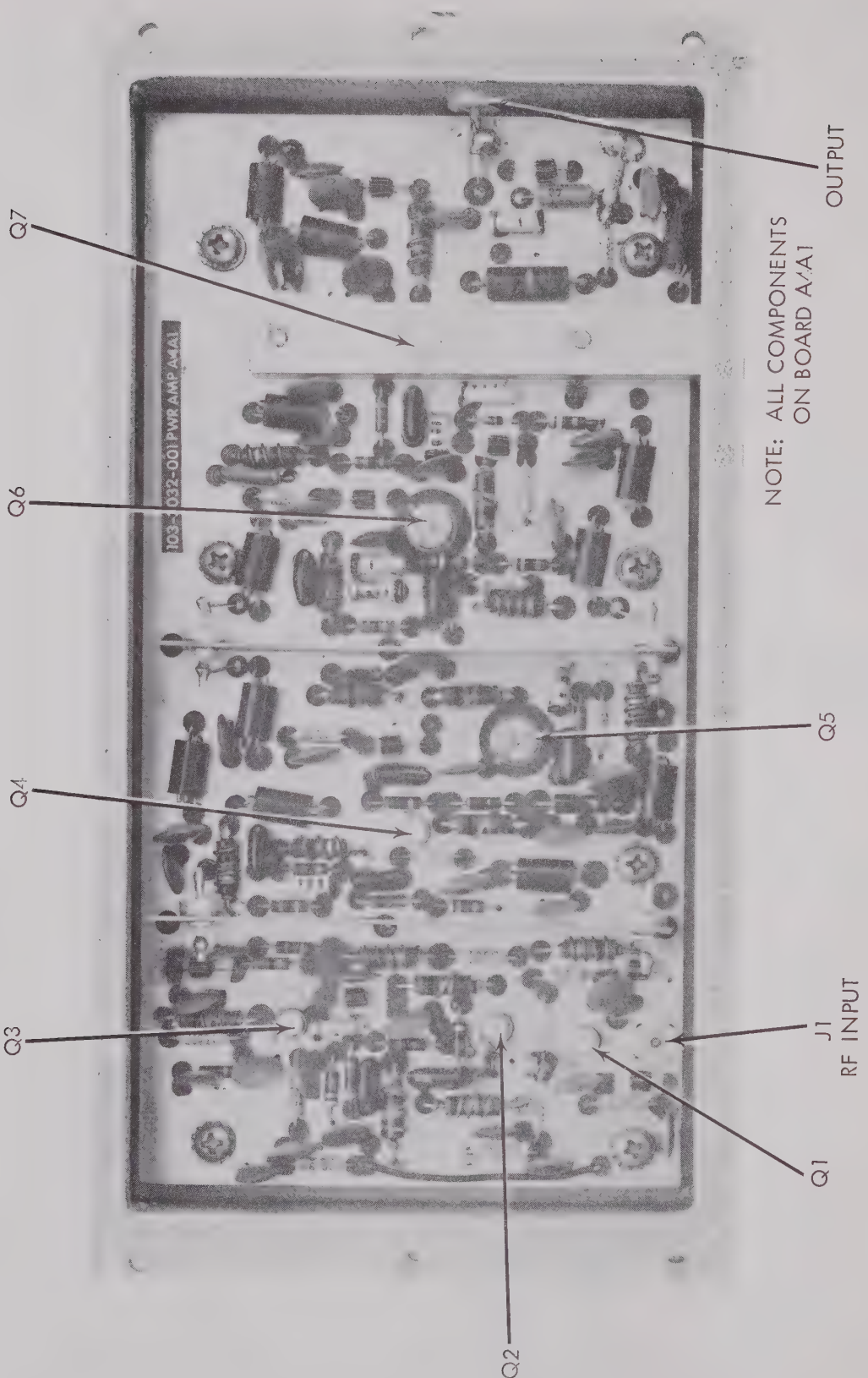


Figure 4-7. Wideband Power Amplifier **A4**

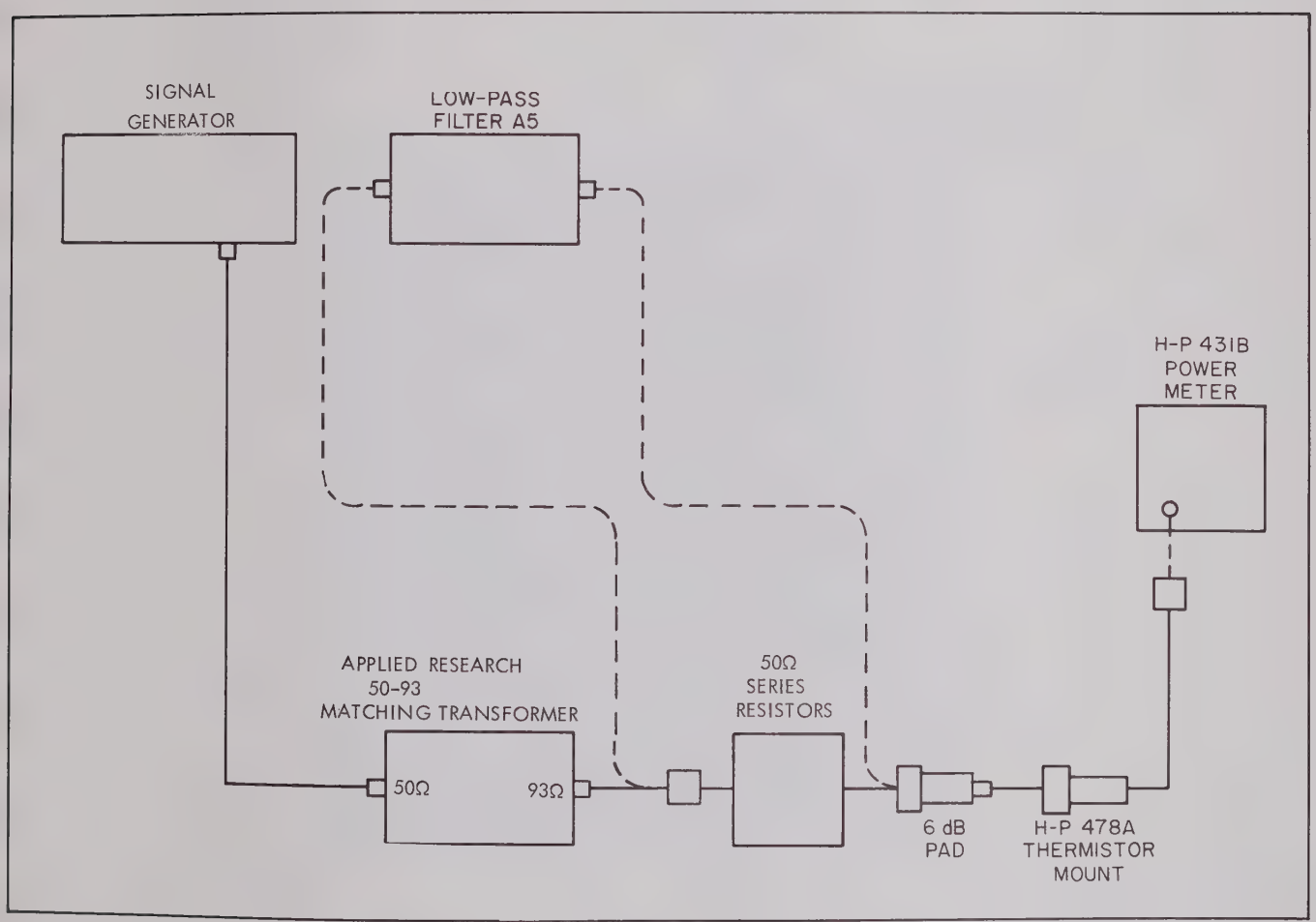


Figure 4-8. Equipment Setup for Low-Pass Filter Checkout

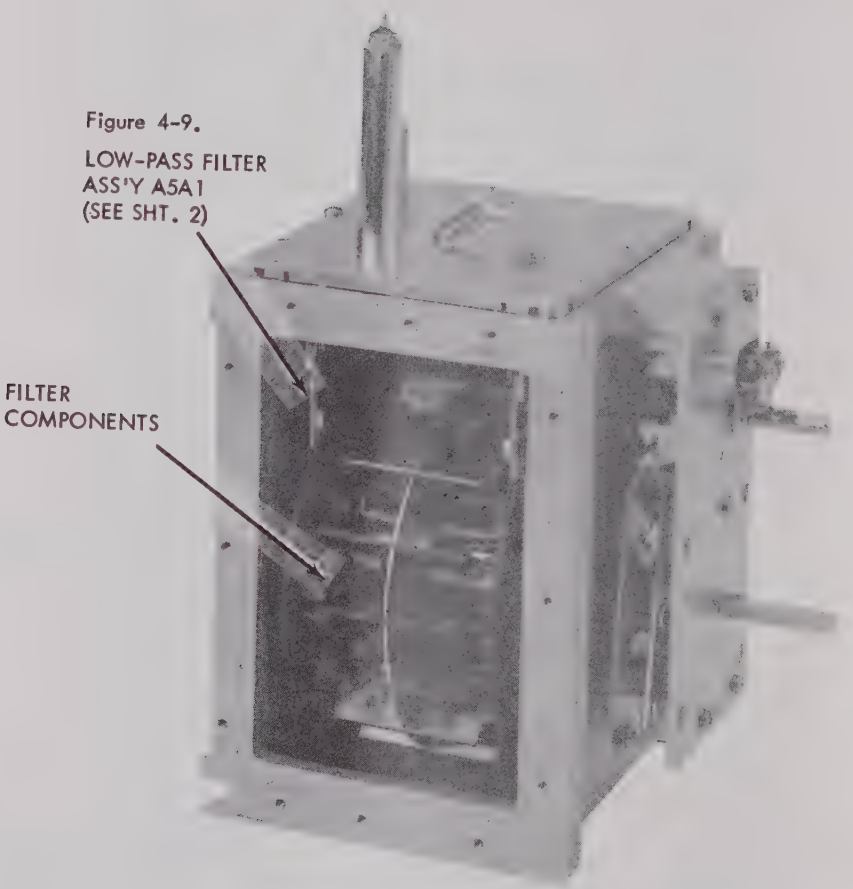


Figure 4-9. Low Pass Filter Assembly A5 (Sheet 1 of 2)

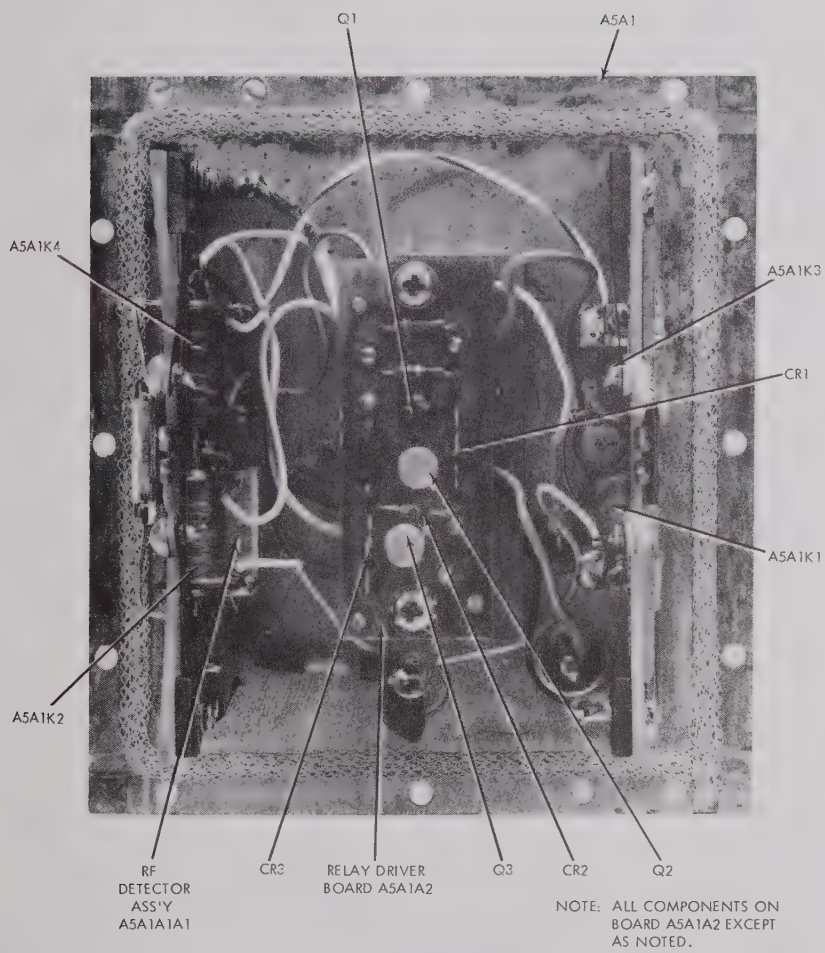


Figure 4-9. Low-Pass Filter Assembly **A5** (Sheet 2 of 2)

4-34. Band Logic Outputs. Place the EXT COUNT pushbutton in the released position. Using a Ballantine Model 355 Digital Voltmeter, ascertain that the proper output voltages are provided at the terminals of A5A3IC1 as a function of RANGE MHz switch and FM CAL pushbutton (refer to Table 4-6).

TABLE 4-6. BAND LOGIC OUTPUT LEVELS

RANGE MHz Switch Setting	Test Point			
	A5A3IC1-3	A5A3IC1-6	A5A3IC1-8	A5A3IC1-11
248-512	1	1	1	1
124-256	0*	1	1	1
62-128	1	0*	1	1
31-64	1	1	0*	1
15.5-32	0*	1	0*	1
7.75-16	1	0*	0*	1

Notes: 1 ("high") level is +2.4 volts or greater
0 ("low") level is between 0 and +0.4 volts

* 1 level when FM CAL pushbutton is pressed

4-35. Frequency Lock Flip-Flop Outputs. Connect a Ballantine Model 355 Digital Voltmeter to terminal 8 of A5A3IC2 (LOCK command output). With the EXT COUNT pushbutton in the released position, momentarily set the NORMAL/LOCK switch to the NORMAL position. A level of between 0 and +0.4 volts DC should be observed on the digital voltmeter and the LOCK indicator should not be lit. Then, momentarily set the NORMAL/LOCK switch to the LOCK position. A level of +2.4 volts DC (or greater) should be observed on the digital voltmeter and the LOCK indicator should be lit. Change the position of the RANGE MHz selector switch or press the EXT COUNT on FM CAL pushbutton and observe that the LOCK indicator goes out.

4-36. OUTPUT ATTENUATOR **A6**

4-37. The output attenuator assembly consists of two sections; a 0 to 80 dB step attenuator (A6A1) and a 0 to 70 dB step attenuator (A6A2). Prior to checking these assemblies, ascertain that the proper operating voltages are being applied (refer to Table 4-4).

4-38. 0 to 80 dB Step Attenuator A6A1.

a. Perform steps a through d of paragraph 4-153 and slide A6A1 toward the rear of the main frame.

b. Using a voltmeter set to the 10 VDC range, measure voltage at the 80 dB eyelet on lamp board A6A1A1 for each position of the attenuator dBm switch. There should be +6 VDC present at the switch positions as indicated in Table 4-7. Check the contacts of switch A6A2S3 and/or lamp A6A1A1DS1 if specified voltages are not obtained.

TABLE 4-7. STEP ATTENUATOR CONTROL VOLTAGES

dBm Switch Setting	A6A1A1 Test Point	A6A2A2 Test Point		
	"80 dB" Eyelet	"10 dB" Eyelet	"20 dB" Eyelet	"40 dB" Eyelet
+10/1.0 V	+6 V	+6 V	+6 V	+6 V
0/0.3 V	+6 V	0 V	+6 V	+6 V
-10/.10 V	+6 V	+6 V	0 V	+6 V
-20/.03 V	+6 V	0 V	0 V	+6 V
-30/10 mV	+6 V	+6 V	+6 V	0 V
-40/3 mV	+6 V	0 V	+6 V	0 V
-50/1.0 mV	+6 V	+6 V	0 V	0 V
-60/0.3 mV	+6 V	0 V	0 V	0 V
-70/.10 mV	0 V	+6 V	+6 V	+6 V
-80/.03 mV	0 V	0 V	+6 V	+6 V
-90/10 µV	0 V	+6 V	0 V	+6 V
-100/3 µV	0 V	0 V	0 V	+6 V
-120/0.3 µV	0 V	0 V	+6 V	0 V
-130/.10 µV	0 V	+6 V	0 V	0 V
-140/.03 µV	0 V	0 V	0 V	0 V

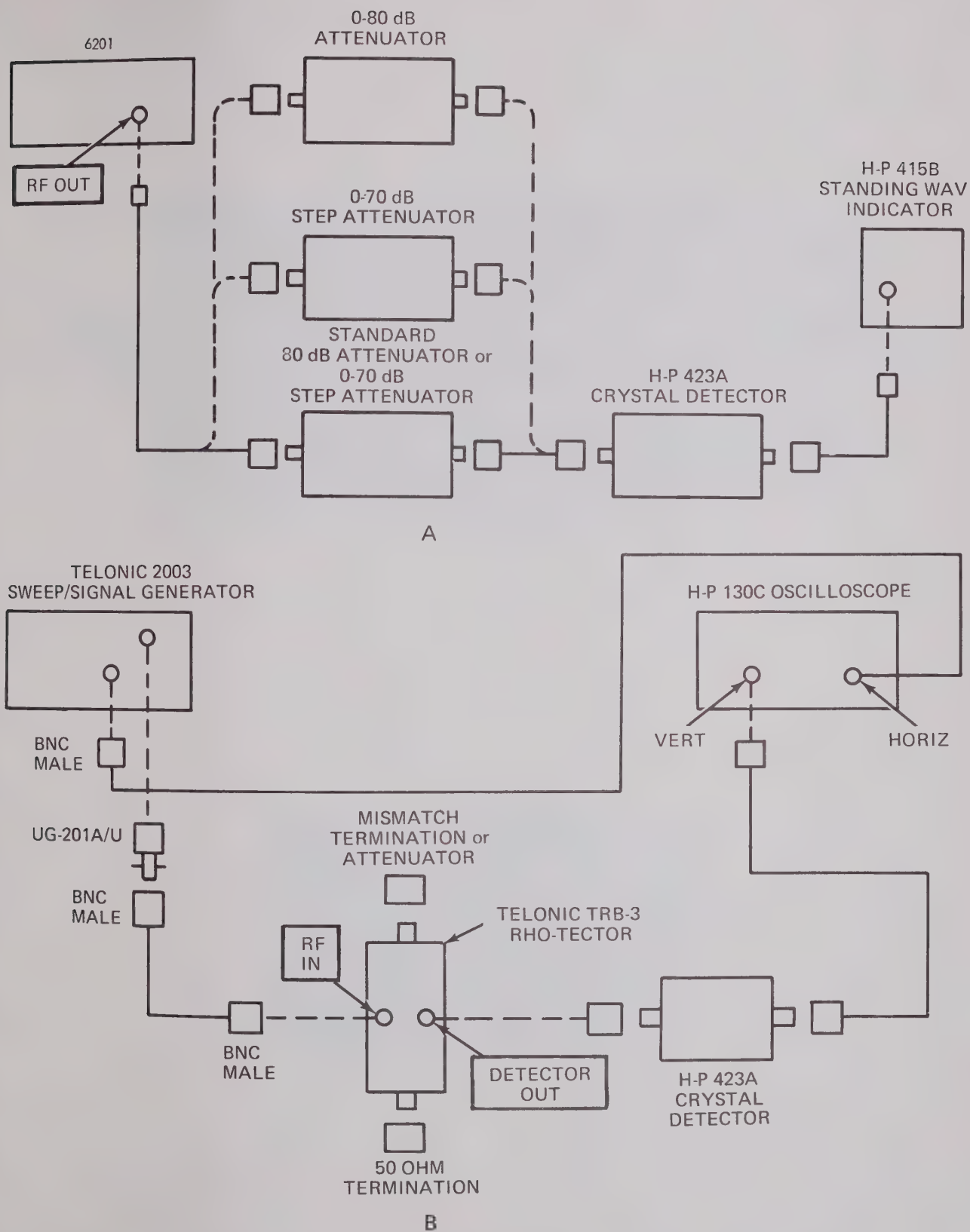
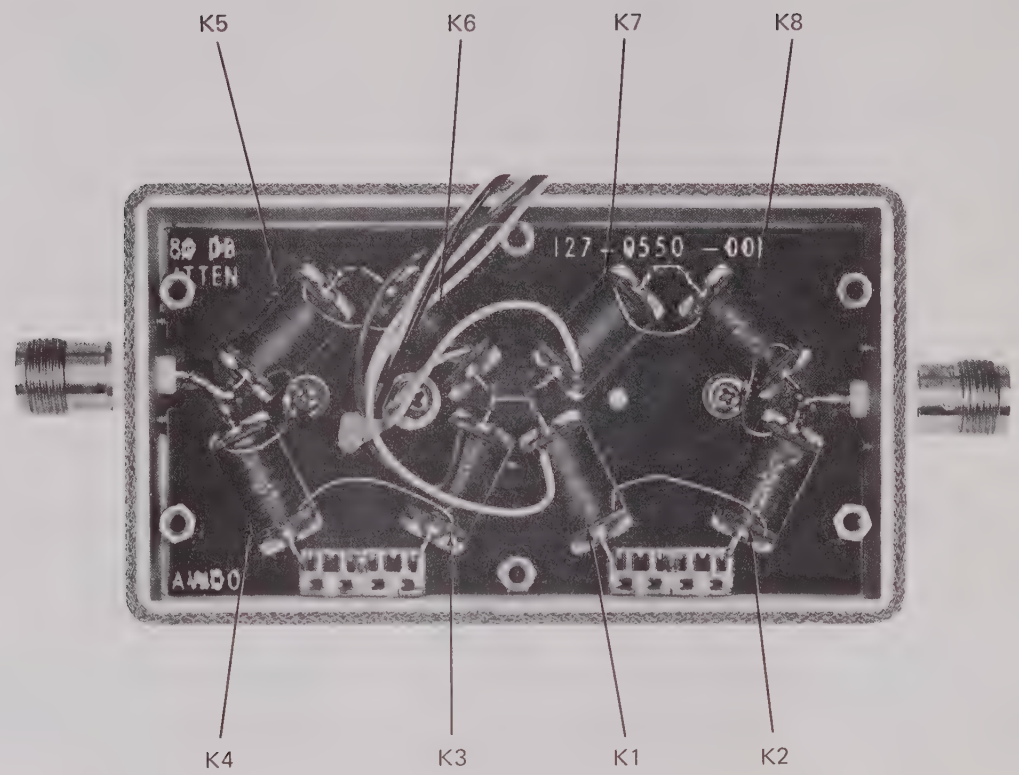


Figure 4-10. Equipment Setup for 0-80 dB and 0-70 dB Step Attenuator Checkout



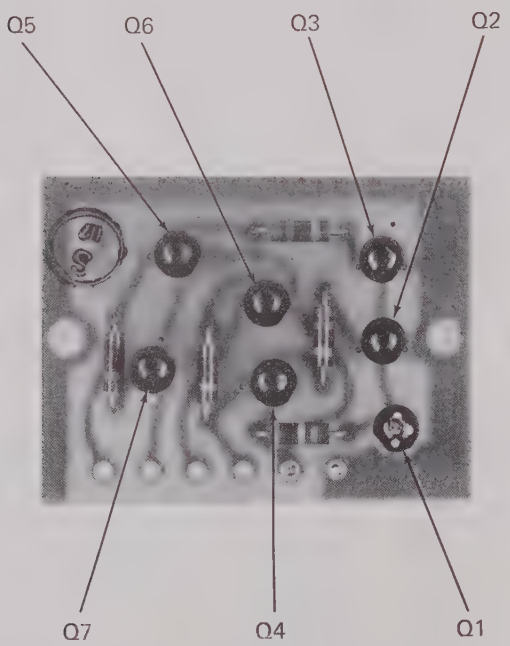
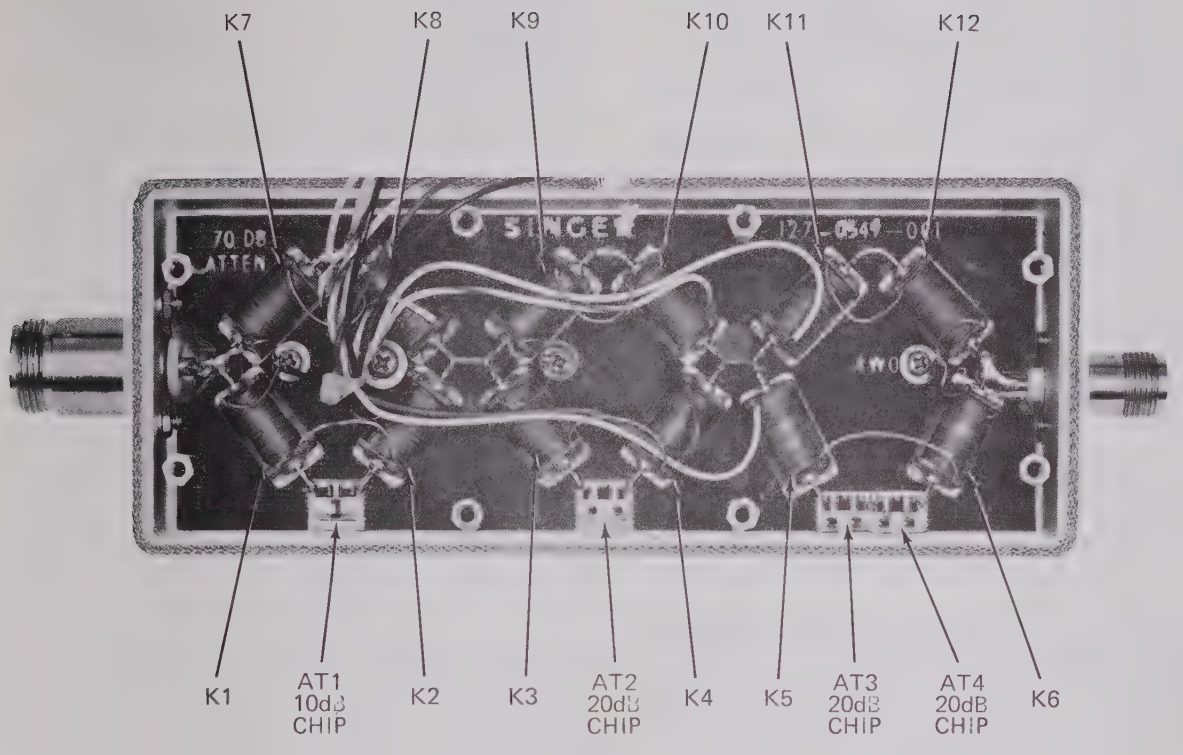


Figure 4-11. 0-80 dB Attenuator A6A1



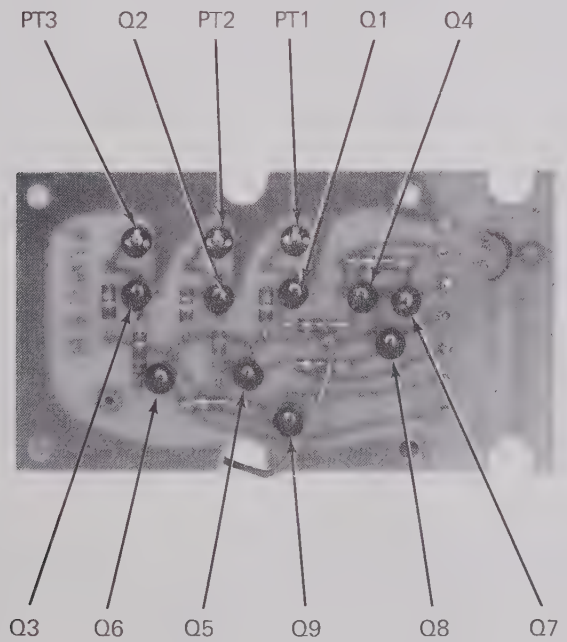


Figure 4-12. 0-70 dB Step Attenuator A6A2

c. Set the attenuator dBm switch to +10/1.0V.

d. Interconnect a standard 80 dB attenuator in the test setup of Figure 4-10A and set the attenuation to 0 dB. Tune the 6201 for a -40 dB output at 10 MHz and 50% AM. Adjust the 6201 modulating frequency to peak the response of the standing wave ratio indicator.

e. Adjust the standing wave indicator to obtain a reference reading of 1 dB on the SWR indicator normal meter scale.

f. Set the dBm switch to +10/1.0V position and connect the 80 dB attenuator under test in the test configuration of Figure 4-10. Note the reading (insertion loss) on the SWR indicator. It should not differ by more than 0.1 dB from the reference.

g. Repeat steps d, e, and f with the 6201 tuned to 500 MHz. Insertion loss should be 0.3 dB maximum at 500 MHz.

h. Set the standard attenuator to its 80 dB position and the dBm switch to -70/.10 mV.

i. Increase the 6201 output to +20 dBm and set the SWR indicator to the 50 dB range.

j. Adjust the SWR indicator for a -1 dB reference reading on the normal scale.

k. Connect the 80 dB attenuator under test in place of the standard attenuator and note the SWR indicator reading. It should be 80 dB ±0.7 dB.

l. Repeat steps i, j, and k with the 6201 tuned to 10 MHz. Attenuation should be 80 dB ±0.7 dB.

m. Malfunctions of this assembly can be located by reference to the assembly schematic diagram in conjunction with the voltage data furnished in Table 4-16. Component locations are shown in Figure 4-11.

4-39. 0-70 dB Step Attenuator.

a. Perform steps a, b, d and e of paragraph 4-152. Slide A6A1 towards the rear of the main frame.

b. Using a voltmeter set to the +10 VDC range, measure voltage at the 10 dB, 20 dB, and 40 dB eyelets on lamp board A6A2A2. There should be +6 VDC present at the dBm switch positions as indicated in Table 4-7. Check the contacts of switches A6A2S1 and A6A2S2 and/or lamp A6A2A2DS1, DS2 or DS3 if specified voltages are not obtained.

c. Interconnect a Telonic 2003 sweep generator, Telonic TRB-3 Rho-tector, H-P 423A detector and H-P 130C oscilloscope as shown in Figure 4-108. Affix the standard 1.25:1 mismatch termination and 50 ohm termination on the Rho-tector as shown in the figure.

d. Adjust the sweep generator and oscilloscope for a full-scale swept VSWR display. Note the 1.25:1 VSWR point.

e. Connect the output connector on the 0-70 dB step attenuator in place of the mismatch termination and terminate the input connector with 50 ohms.

f. Set the attenuator dBm switch to the +10/1.0V (0 dB), 0/0.3V (10 dB), -10/.10V (20 dB) and -30/10 mV (40 dB) positions and note the VSWR indication on the oscilloscope. It should be 1.25:1 maximum for all positions.

g. Repeat steps f and g with the 0-70 dB attenuator input connected in place of the mismatch termination. Terminate the output connector with 50 ohms. VSWR should be 1.25:1 maximum for all positions.

h. Perform step d of paragraph 4-38, except substitute a standard 0-70 dB step attenuator.

i. Adjust the standing wave ratio indicator gain to obtain a reference reading of -0.5 dB on the expanded meter scale.

j. Set the step attenuator under test for 0 dB (dBm switch at +10/1.0V) and connect it in place of the standard 0-70 dB attenuator. Note the reading (insertion loss) on the SWR indicator. It should not differ by more than 0.1 dB.

k. Repeat step j, setting the attenuator dBm switch, SWR indicator range and/or 6201 output level as indicated in Table 4-8 and note the SWR reading.

NOTE

Adjust the 6201 output and/or the SWR indicator range as necessary to maintain the 0.5 dB reference reading.

l. Set the 6201 to 500 MHz and repeat steps i through k. The same accuracy should be obtained.

m. Malfunctions of this assembly can be located by reference to the assembly schematic diagram in conjunction with the voltage data furnished in Table 4-16. Component locations are shown in Figure 4-12.

TABLE 4-8. 0-70 dB STEP ATTENUATOR CHECKOUT

dBm Switch Setting	SWR Indicator "Range" Switch Setting	6201 Signal Generator Output Level	SWR Indicator Reading (max)*
1/0.3 V	40	-40 dBm	1 ±0.15 dB
-10/.10 V	20	-20 dBm	1 ±0.30 dB
-20/.03 V	30	-20 dBm	1 ±0.45 dB
-30/10 mV	40	-20 dBm	1 ±0.60 dB
-40/3 mV	20	0 dBm	1 ±0.75 dB
-50/1.0 mV	30	0 dBm	1 ±0.90 dB
-60/0.3 mV	40	0 dBm	1 ±1.05 dB

* Maximum cumulative error should not exceed ±1.05 dB.

4-40. MODULATION AND SWITCHING ASSEMBLY A7.

4-41. A malfunction within this assembly can be located using signal tracing techniques in conjunction with the information provided in Table 4-7. To gain access to assembly A7, perform steps a and e of paragraph 4-155 and then carefully slide the counter assembly back and turn it over so that the assembly rests on low-pass filter assembly A5. The locations of the components on A7 are shown in Figure 4-13.

4-42. FREQUENCY COUNTER A8

4-43. To check assembly A8 for proper operation, first remove the assembly as described in paragraph 4-155, disassemble it as described below and then perform the checks of paragraphs 4-44 and 4-45. Refer to paragraph 4-46 for limited troubleshooting of the counter. The locations of components on A8 are shown in Figure 4-14.

a. Remove the three screws on the top and the six screws on the bottom of the assembly, and gently remove the case from A8.

b. Remove the three screws which fasten the printed circuit board retainer plate to the assembly.

CAUTION

To prevent possible damage to assembly A8, mount it on a sheet of paper or plastic before performing step c.

c. Reconnect A8 to the Signal Generator as follows: connect multipin connector A8P2 to A5A3J2; connect P7, P10 and P11 to A8A1J2, A8A1J4 and A8A1J5, respectively; and connect W2P2 and W3P1 to A8A1J3 and A8A1J1, respectively.

d. Check that the proper voltages are being applied to A8 (refer to Table 4-4).

4-44. Frequency Counter Time Base Accuracy.

a. Set the rear-panel INT TIME BASE switch to 1 sec and press the front-panel EXT COUNT pushbutton.

b. Couple the 10 MHz time base output of an H-P 5245L frequency counter to the front-panel EXT COUNT connector.

c. Adjust trimmer capacitor A8A3A6C8 until the frequency display readout of the Signal Generator indicates 000.000 kHz.

NOTE

The Signal Generator top cover should be removed for as short a time as possible when adjusting the frequency of 4 MHz oscillator A8A3A6Q8.

4-45. Band Center Switching.

a. Connect a Tektronix 585 oscilloscope (DC coupled) to A8A1FL6 (BAND CTR CMD).

b. Set the RANGE MHz selector switch to 7.75 to 16 MHz. While observing the oscilloscope, go up and down the 7.75 to 16 MHz frequency range. The voltage on A8A1FL6 should go to zero volts at 10.9000 MHz ±20 kHz going down frequency and should go to approximately +4 volts at 11.1000 MHz ±5 kHz going up in frequency. If not, perform the adjustments of steps d through g.

c. Connect the Tektronix 585 oscilloscope (AC coupled) to A8A1FL7 (BAND CTR PULSE). The output on A8A1FL7 should be a positive pulse when the voltage at A8A1FL6 changes from zero to approximately +4 volts or from approximately +4 volts to zero.

d. Turn trigger adjust potentiometer A8A3A6R2 and hysteresis adjust potentiometer A8A3A6R1 fully clockwise.

e. Set the Signal Generator frequency to 10.9000 MHz. The voltage on A8A1FL6 should be approximately +4 volts. Slowly adjust trigger adjust potentiometer A8A3A6R2 until this voltage goes to zero.

f. Set the Signal Generator frequency to 11.1000 MHz. Slowly adjust hysteresis adjust potentiometer A8A3A6R1 until the voltage on A8A1FL6 goes to +4 volts.

g. Repeat step b.

4-46. Counter Troubleshooting Techniques and Checkout. As with all sophisticated digital electronic equipment, troubleshooting techniques that may be applied to the frequency counter can vary considerably. In the suggested technique, a test frequency is inserted and logic states throughout the counter circuits are monitored and compared with the "normal" states for the test frequency. This signal tracing technique requires a detailed knowledge of the logical operations performed. An oscilloscope is used to monitor the logic states. The theory of operation presented in Section III and in this section describes the logical operations in detail and also provides tables of logic states at selected functional output points for each frequency band.

4-47. Table 4-9 provides a checkout procedure for localizing malfunctions to a printed circuit board level within A8A3. The circuit board may be replaced or additional troubleshooting conducted using the signal tracing technique described above in conjunction with "normal" voltage measurements at transistors, etc., furnished in Table 4-18. Proceed as follows:

a. With A8 removed from the Signal Generator, disassemble A8 as described in steps a through c of paragraph 4-43. Install the printed circuit board to be tested on a board extender.

NOTE

The Signal Generator is used as the frequency source for the checkout procedures.

b. If the counter is inoperative on all frequency bands, set the Signal Generator to approximately 248 MHz (the low end of the 248-512 MHz band). The exact frequency is not important. Follow the checkout procedure for an inoperative counter in Table 4-9.

c. If the malfunction exists on two or more bands, but not on all, set the Signal Generator to the low end of an

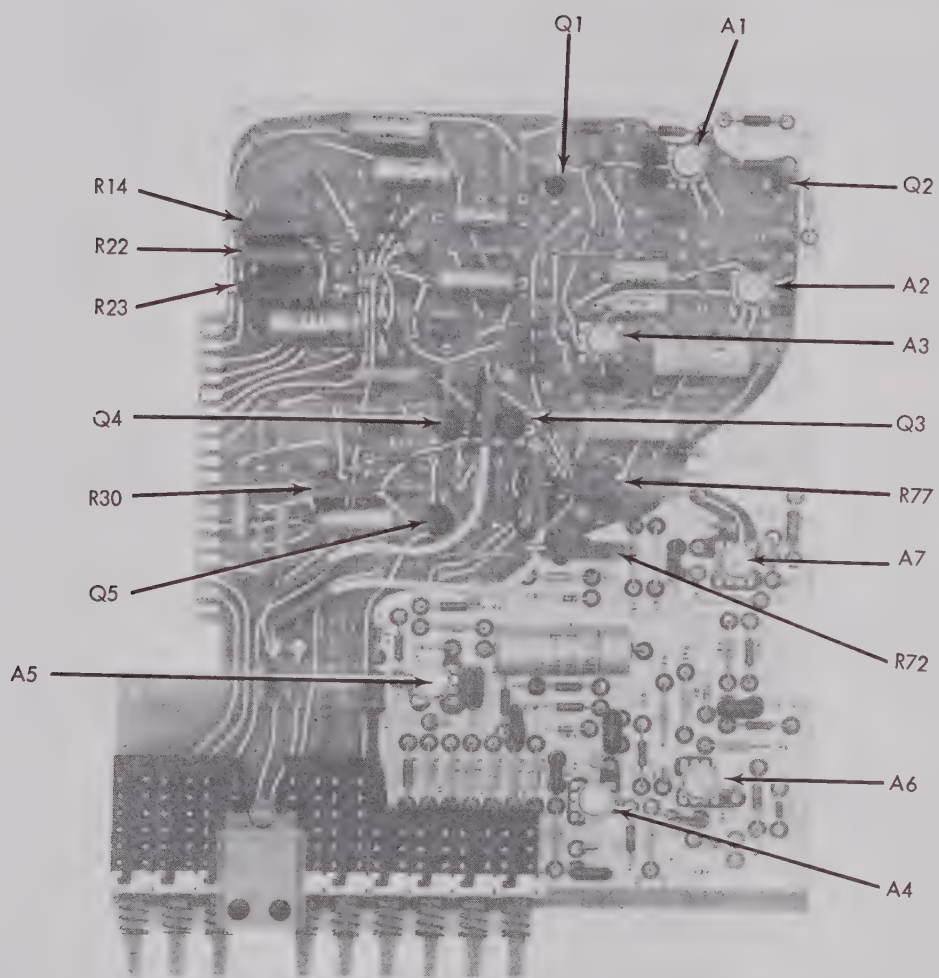


Figure 4-13. Modulation and Switching Assembly A7

Figure 4-14. Frequency Counter **A8** (Sheet 1 of 7)

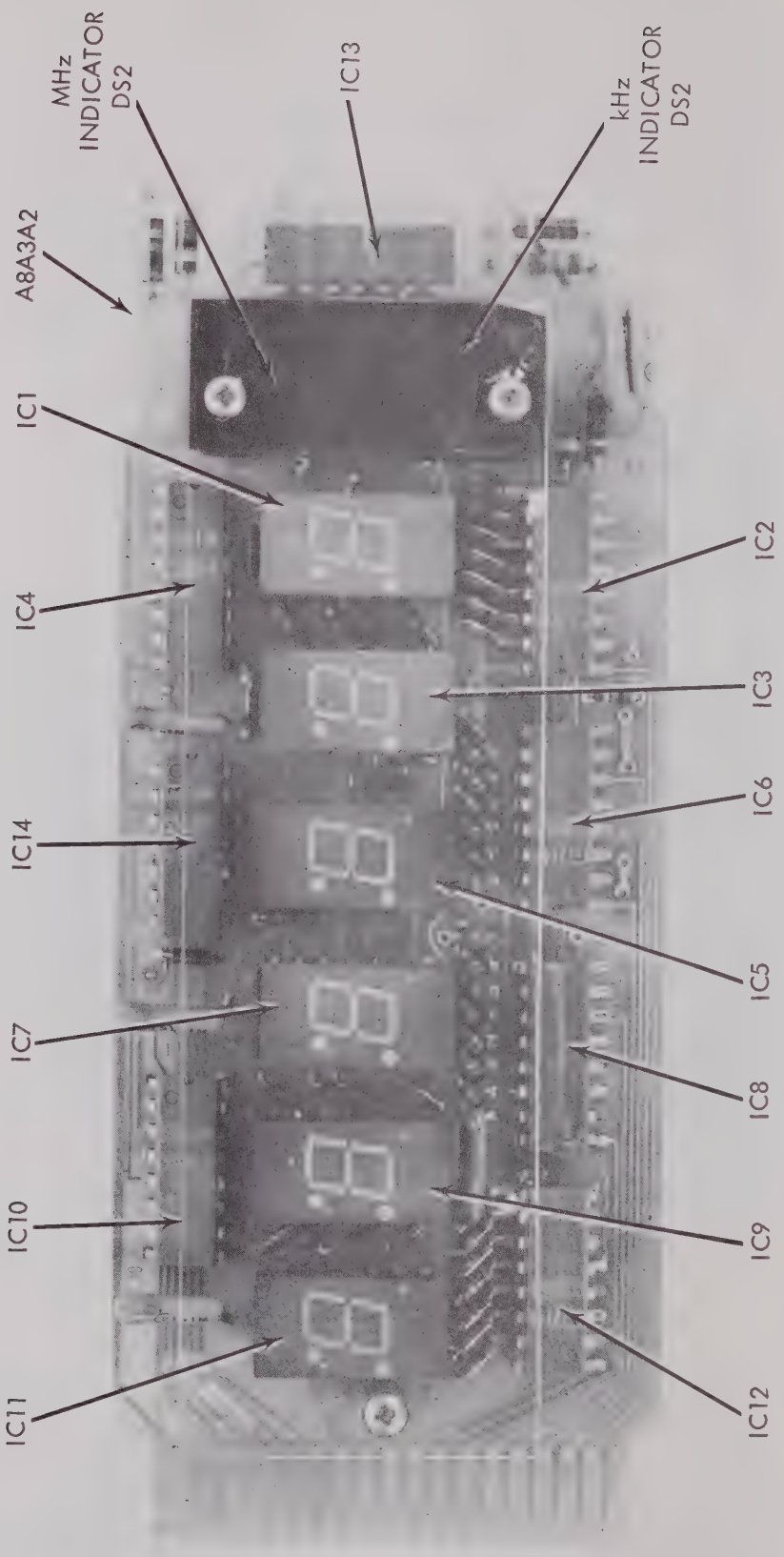


Figure 4-14. Frequency Counter **A8** (Sheet 2 of 7)

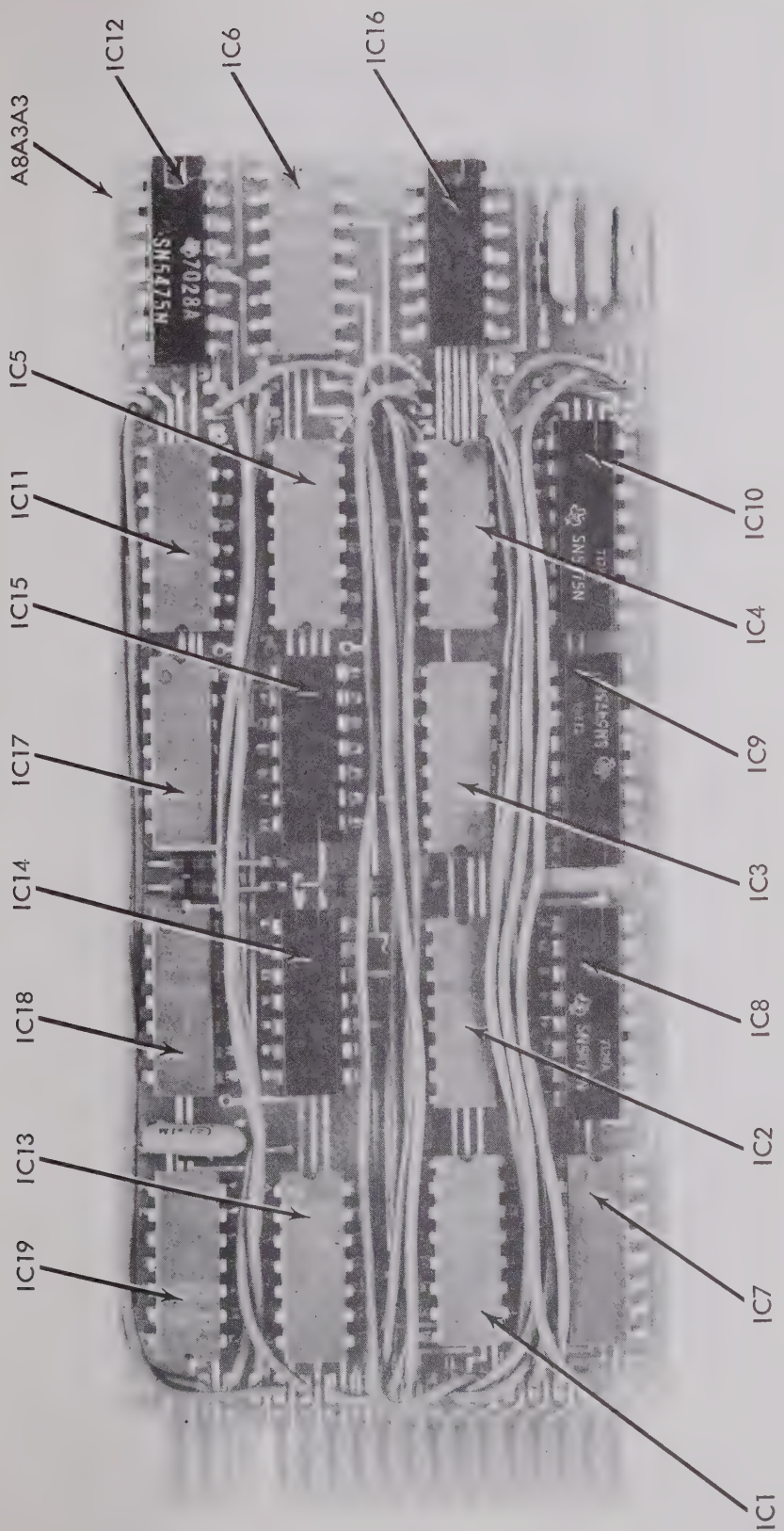


Figure 4-14. Frequency Counter **A8** (Sheet 3 of 7)

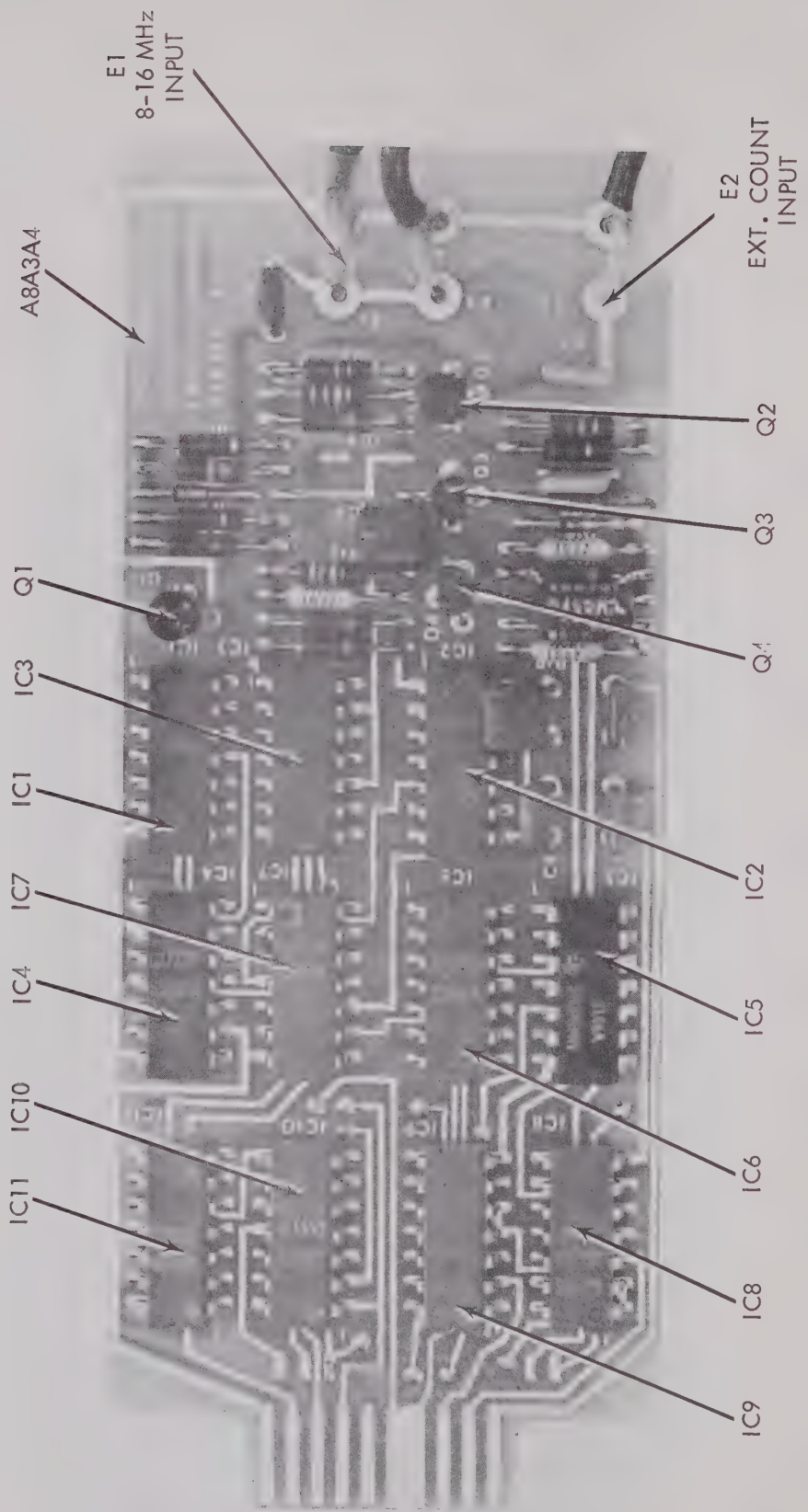


Figure 4-14. Frequency Counter A8 (Sheet 4 of 7)

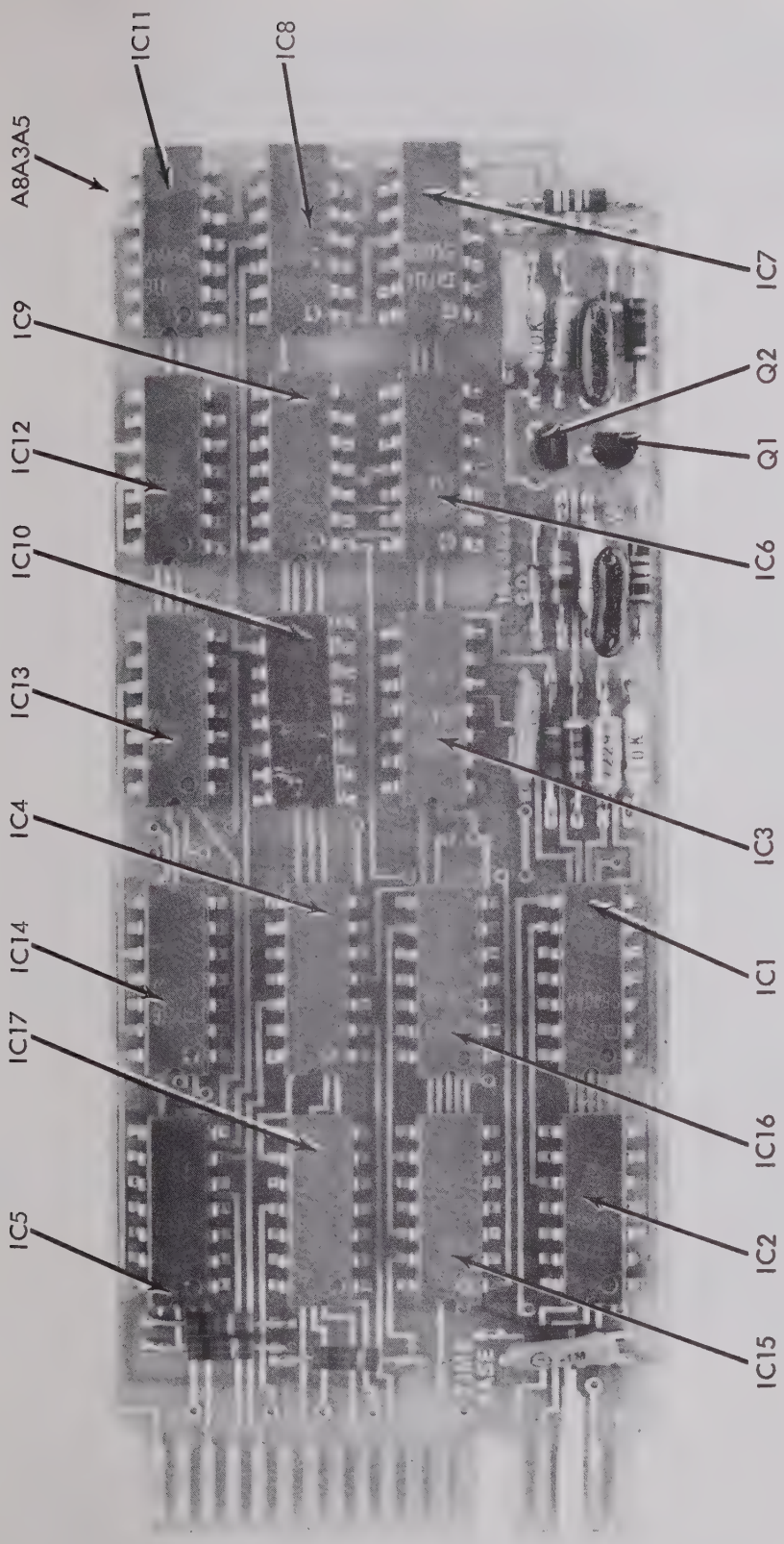


Figure 4-14. Frequency Counter **A8** (Sheet 5 of 7)

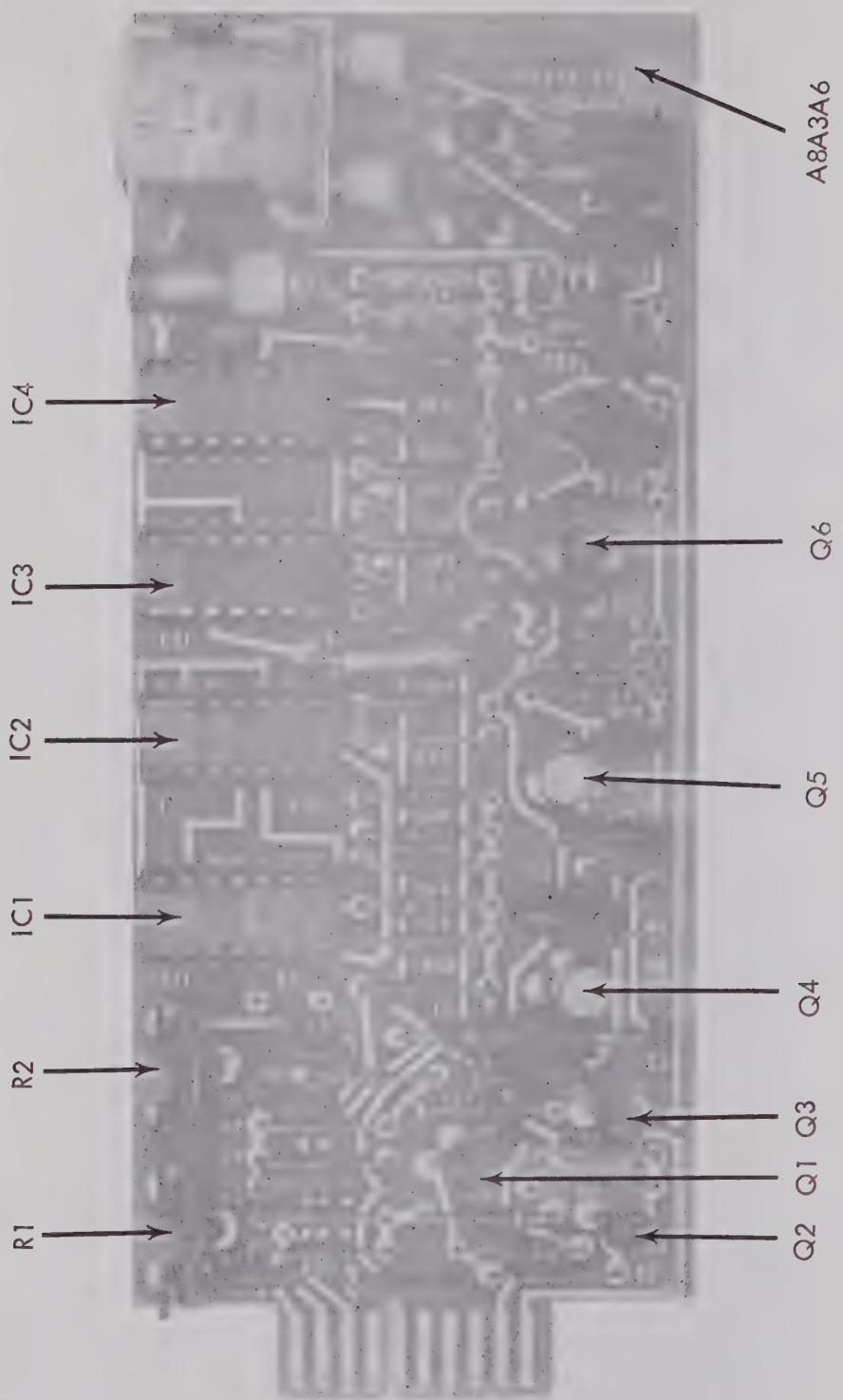


Figure 4-14. Frequency Counter **A8** (Sheet 6 of 7)

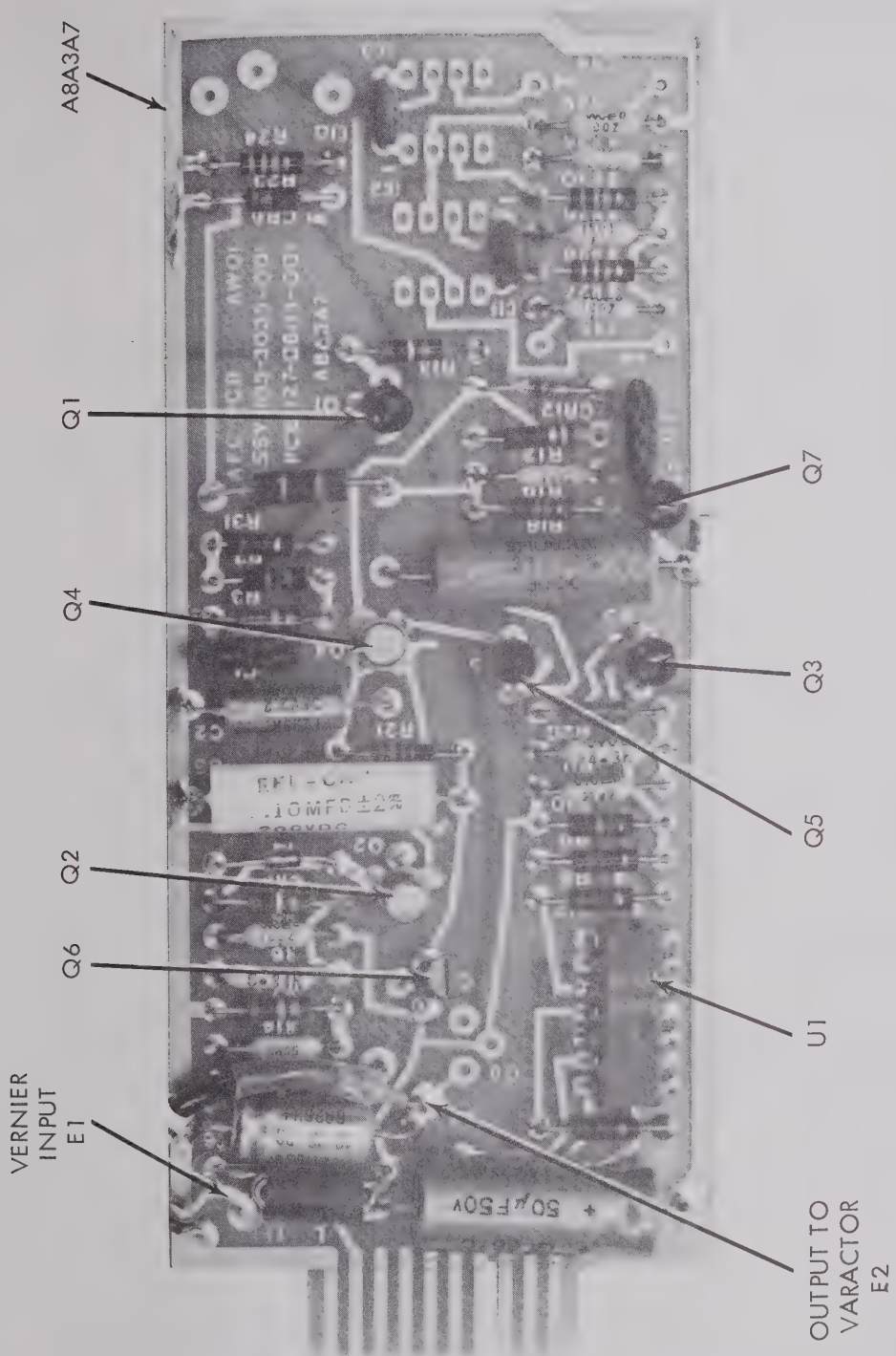


Figure 4-14. Frequency Counter **A8** (Sheet 7 of 7)

TABLE 4-9. FREQUENCY COUNTER A8 CHECKOUT

Step	Procedure	Normal Indication	If Indication is Abnormal
Inoperative on all Frequency Bands.			
1	Connect an electronic counter and/or oscilloscope to monitor the 1 MHz clock output at oscillator board A8A3A6, pin 3.	1 MHz clock pulses, > +2.4 volt amplitude. Proceed to step 2.	Oscillator board A8A3A6 is defective.
2	Using an oscilloscope or digital voltmeter, check the following logic inputs to time base board A8A3A5: a. $\overline{A} + B$ at pin 10. b. $\overline{A} \cdot B$ at pin 9. c. CS at pin 4. d. DS at pin J.	a. > +2.4 volts b. 0 to +0.4 volts. c. > +2.4 volts. d. > +2.4 volts. Proceed to step 3.	If any of the inputs are abnormal, pre-scaler board A8A3A4 is defective.
3	Check the following pulse/logic outputs from time base board A8A3A5: a. ΔT gate at pin 7. b. STORE command at pin L. c. CLEAR command at pin P. d. $\overline{\text{LOOP MODE}}$ at pin 5.	a. 256 msec ΔT gate. See Figure 4-29. b. See Figure 4-29. c. See Figure 4-29. d. > +2.4 volts. Proceed to step 4.	If any of the outputs are abnormal, time base board A8A3A5 is defective.
4	Monitor the F_C pulse output at pre-scaler board A8A3A4, pin 6.	970 kHz pulses (approx.) > +2.4 volt amplitude. Proceed to step 5.	Pre-scaler board A8A3A4 is defective.
5	Check the 4-bit BCD inputs (24 lines) to display board A8A3A2, at applicable pins (see display circuitry schematic, Figure 4-26). **NOTE** If normal indications are obtained in steps 1 through 5, display board A8A3A2 is defective.	Logical ONE (> +2.4 volts) and ZERO (0 to +0.4 volts) levels; refer to Table 3-2.	Counter/storage board A8A3A3 is defective.
Inoperative on Bands 1 through 3 only.			
6	Monitor the CS logic input to the time base board A8A3A5, pin 4.	> +2.4 volts. Proceed to step 7.	Pre-scaler board A8A3A4 is defective.
7	Check the ΔT gate output from time base board A8A3A5, pin 7.	256 msec ΔT gate. See Figure 4-29.	Time base board A8A3A5 is defective.

TABLE 4-9. FREQUENCY COUNTER A8 CHECKOUT (CONTINUED)

Step	Procedure	Normal Indication	If Indication is Abnormal
Inoperative on Bands 4 through 6 only. 8	Monitor the CS logic input to time base board A8A3A5, pin 4.	0 to +0.4 volts. Proceed to step 9.	Pre-scaler board A3A3A4 is defective.
Inoperative on Bands 1 through 4 only. 9	Check the ΔT gate output from time base board A8A3A5, pin 7.	320 msec ΔT gate. See Figure 4-29.	Time base board A8A3A5 is defective.
Inoperative on Bands 2 and 5 only. 10	Set the Signal Generator to 248 MHz or 31 MHz. Monitor the F_c pulse output at pre-scaler board A8A3A4, pin 6.	970 kHz pulses (approx.), > +2.4 volt amplitude.	Pre-scaler board A8A3A4 is defective.
Inoperative on Bands 3 and 6 only. 11	Set the Signal Generator frequency to 124 MHz or 15.5 MHz. Monitor the F_c pulse output at pre-scaler board A8A3A4, pin 6.	485 kHz pulses (approx.), > +2.4 volt amplitude.	Pre-scaler board A8A3A4 is defective.
Inoperative in frequency lock mode only. 12	Set the Signal Generator frequency to 62 MHz or 7.75 MHz. Monitor the F_c pulse output at pre-scaler board A8A3A4, pin 6.	242 kHz pulses (approx.), > +2.4 volt amplitude.	Pre-scaler board A8A3A4 is defective.
13	Set the Signal Generator frequency to 248 MHz. Check the following outputs from time base board A8A3A5: a. DOWNGATE command at pin C. b. Reference square wave at pin F.	a. > +2.4 volts. b. 63 Hz pulses (approx.) > +2.4 volt amplitude. Proceed to step 14.	If any of the outputs are abnormal, time base board A8A3A5 is defective.

TABLE 4-9. FREQUENCY COUNTER A8 CHECKOUT (CONTINUED)

Step	Procedure	Normal Indication	If Indication is Abnormal
14	Check the ZERO count pulse at AFC board A8A3A7, pin F. **NOTE** If normal indications are obtained in steps 13 and 14, AFC board A8A3A7 is defective. **NOTE** If operation is normal on all but the external count mode, pre-scaler board A8A3A4 is probably defective.	1.2 msec pulses, > +2.4 volt amplitude.	Counter/storage board A8A3A3 is defective.
Inoperative in external count mode only.			

4-48. DETAILED CIRCUIT DESCRIPTION.

4-49. A detailed circuit description for each of the functional blocks of the Signal Generator precedes the respective functional schematic diagram.

4-50. FREQUENCY GENERATION CIRCUITRY. Figure 4-15.

4-51. 248 - 512 MHz Master Oscillator. UHF transistor A1A1Q1 is a common-base amplifier with positive feedback. The collector of Q1 is connected to the center conductor of a 1/4-wave length resonant coaxial cavity which determines the frequency of oscillation. The front-panel FREQUENCY control tunes the oscillator over the 248 to 512 MHz frequency range by changing the physical length of the cavity with a movable ceramic slug. Electronic fine tuning (over a range of at least 300 ppm) is achieved by means of varactor A1CR1, which alters the electrical length of the coaxial line by effectively changing the capacitance at the end of the cavity. Loop coupling is employed at the shorted end of the coaxial cavity to extract the master oscillator output power level of approximately 2 milliwatts (+3 dBm).

4-52. Frequency Divider. The following subparagraphs describe the stages of the frequency divider.

4-53. Band 1 Amplifier A2A1. The basic 248 to 512 MHz output of master oscillator A1 is applied through A2P1 and transformer-coupled to both the emitter of A2A1Q1, the first stage of a saturating buffer amplifier, and the emitter of isolation amplifier A2A1Q2. Saturating buffer A2A1Q1 and A2A1Q5 boosts the level of the master oscillator signal to approximately 5 milliwatts, a level sufficient to drive band 2 frequency divider A2A2A1, the first stage of a five stage binary frequency divider chain. In addition to providing both the leveling action and drive for the following binary divider, the saturated buffer amplifier also provides approximately 80 dB of isolation between the first frequency divider and isolation amplifier A2A1Q2, thereby eliminating divider-generated subharmonics from appearing at the output when the RANGE MHz switch is set to 248 - 512 (band 1).

4-54. Band 2 Frequency Divider A2A2A1 and Band 3 Frequency Divider A2A2A2. These two frequency dividers are identical except for frequency-dependent component values. The drive signal from the preceding stage is applied to toggle transistors Q1 and Q2, a high-speed banary divider. The divided frequency output appears at each collector. The output at the collector of Q2 is coupled through a two stage isolation amplifier (Q3 and Q4) which serves a three-fold function: it amplifies the divided signal to a level suitable to drive the following divider stage; it filters the output waveform to provide a relatively clean sinusoidal output; and it provides the necessary isolation to prevent f/2 leakage signals from the following stage.

4-55. Since the output of the master oscillator is greater than one octave and the divider outputs contain harmonic distortion products, low-pass filters with switchable upper cutoff frequencies are placed in the divider output path. Each filter consists of capacitors C1 through C3, inductor L1 and diode CR1. When the output frequency of master oscillator A1 is below the geometric mean of its range (355 MHz), the band center command voltage applied to the base of inverter A2A1Q3 is 0 volts. The transistor is therefore cutoff and switch A2A1Q4 is saturated, causing diode CR1 to conduct. Bridging capacitor C2 is in the circuit and the cutoff frequency of the filter is just above the geometric mean of the band. The filter attenuates unwanted harmonic products of the divided signal developed at the collector of Q1, thereby providing a clean sinusoidal output to drive the modulator.

4-56. Similarly, when the master oscillator output frequency is above the geometric mean, the band center command voltage applied to the base of A2A1Q3 is +5 volts. Switch A2A1Q4 is cutoff, preventing diode CR1 from conducting, thereby removing bridging capacitor C2 from the filter. This action causes the cutoff frequency of the filter to be shifted slightly above the high end of the band, while maintaining a steep skirt, to again provide a clean output waveform for driving the modulator.

4-57. Band 4 Frequency Divider A2A2A3, Band 5 Frequency Divider A2A3A1 and Band 6 Frequency Divider A2A3A2. The 62 to 128 MHz output of the band 3 frequency divider is applied to A2A2A3MC1, an integrated circuit binary divider. One output of the divider is coupled through isolation amplifier A2A2A3Q1 to the band 5 divider while the other output is coupled to A2A1S1. The band 4, 5 and 6 frequency dividers are similar, with the one following exception: the band 6 divider has three outputs. One output is applied to switch A2A1S1, the second output (at A2J3) is coupled to the optional plug-in frequency extender module and the thrid output (at A2J2) is applied to the frequency counter. Note that, unlike the band 2 and 3 frequency dividers, the band 4, 5 and 6 frequency dividers do not have low-pass filters in the output path to switch A2A1S1.

4-58. The output of isolation amplifier A2A1Q2 and the outputs of each subsequent frequency divider, all being typically -10 dBm, are coupled to a high-isolation printed circuit type RF switch, A2A1S1. This switch, whose position is determined by the setting of the RANGE MHz control, routes the output of the band 1 amplifier or any one of the five divider outputs to the following stage.

4-59. BALANCED MODULATOR AND LEVEL CONTROL CIRCUITRY. Figure 4-16.

4-60. Wideband Preamplifier. RF amplifiers A3A2A1Q1 and A3A2A1Q2 increase the frequency divider output (7.75 to 512 MHz) by approximately 15 dB. High-frequency series compensation is provided by coils A3A2A1L2 and A3A2A1L4; low-frequency compensation is provided by capacitors A3A2A1C10 and A3A2A1C14. Degenerative feedback from the emitter of Q2 to the base of Q1 (through R4) provides the wideband preamplifier with a low input VSWR over its operating range. The low input VSWR presents a reasonably constant output impedance to the frequency divider, particularly in bands 2 and 3, where the low-pass filters depend on a 50-ohm load for proper frequency response. The preamplifier provides a minimum saturated output power level of 1 milliwatt (0 dBm) to the first balanced modulator.

4-61. Balanced Modulators. First balanced modulator A3A2A2 and second balanced modulator A3A2A3 are sealed, non-repairable modules with bandpass characteristics similar to the wideband preamplifier. The insertion loss of the two modulators in series can be varied over a dynamic range of approximately 60 dB. The RF impedance of the diodes within the two modulators is varied via the RF level control circuit as described in paragraph 3-23.

4-62. RF Level Control Circuit. The stages of the circuit are discussed in the following subparagraphs.

4-63. Leveling Amplifier A3A1MC2. This stage is an inverting IC operational amplifier which is connected to the output of adding network A3A1R28, A3A1R29 and A3A1C16. The gain of the amplifier is normally determined by feedback network A3A1R32, A3A1C17; and resistors A3A1R28 and A3A1R29. However, during pulsed operation, P-channel FET A3Q10 is gated on by 0 volts (ground) from switching transistor A3A1Q9, thereby connecting resistor A3A1R35 in the amplifier feedback path. This reduces the DC gain of the amplifier.

4-64. Isolation Amplifier A3A1Q11 and Emitter Followers A3A1Q12 and A13A1Q15. Stage A3A1Q11 is a common-emitter amplifier which increases the output of the preceding leveling amplifier to a level suitable to drive the balanced modulators. Emitter followers A3A1Q12 and A3A1Q15 provide a low-impedance path to the balanced modulators.

4-65. Sample and Hold Circuit. The stages of the sample and hold circuit are discussed in the following subparagraphs.

4-66. Inverters A3A1Q2, A3A1Q4 and A3A1Q5. These three common-emitter amplifiers function as switching transistors. When the Signal Generator is set up for external pulse modulation and no positive modulating signal is present at the input of A3A1Q2, both this transistor and A3A1Q5 are cutoff and A3A1Q4 is saturated. This results in a +12 volts output from A3A1Q5. When a positive modulating signal is applied to A3A1Q2, both it and A3A1Q5 are saturated and A3A1Q4 is cutoff. This results in a 0 volts (ground) output from A3A1Q5. When not in pulsed operation, +12 volts from switching transistor A3A1Q3 places A3A1Q4 at saturation and A3A1Q5 at cutoff, resulting in a +12 volts output from A3A1Q5.

4-67. FET A3A1Q6 and Unity-gain Amplifier A3A1MC1. P-Channel FET A3A1Q6 is gated on by the 0 volts output (ground) of inverter A3A1Q5. When gated on, capacitor A3A1C11 is allowed to charge to the negative output of RF detector A5A1A1 via the saturated FET and resistor A3A1R20. A3A1MC1 is a non-inverting IC operational amplifier which is connected in a voltage follower configuration Feedback resistor A3A1R19 is tied to the inverting input terminal of A3A1MC1.

4-68. WIDEBAND POWER AMPLIFIER CIRCUITRY. Figure 4-17.

4-69. RF amplifiers A4A3Q1 through Q7 increase the second balanced modulator output (7.75 to 512 MHz) by approximately 50 dB. High-frequency series and shunt compensation and low-frequency compensation are used throughout the amplifier chain to obtain the required bandpass. Degenerative feedback from the emitter of Q2 to the base of Q1 (through R3) provides the wideband power amplifier with a low input VSWR over its operating range. The output power level from power amplifier Q7 is greater than +14 dBm (VX2 pushbutton released) or +20 dBm (VX2 pushbutton pressed).

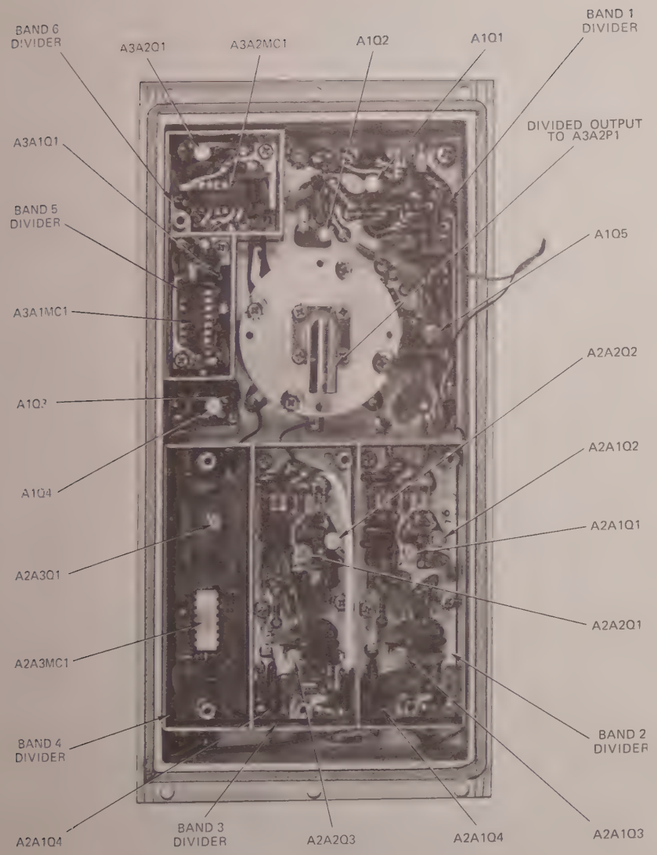
4-70. LOW-PASS FILTER CIRCUITRY. Figure 4-18.

4-71. This circuitry consists of a manually-driven filter selector turret switch (mechanically ganged to the RANGE MHz switch) containing six pairs of low-pass filters, five electronically actuated reed relays, and one magnetically actuated reed relay. When the RANGE MHz switch is set to any position other than PLUG-IN, the output of wideband power amplifier A4 is coupled through A5A1J1 and applied simultaneously to reed relays A5A1K1 and A5A1K3. A band center command voltage, obtained from band center command circuitry (refer to paragraph 4-90) is coupled through R-C RFI filter A5A1A6 to the base of switdh A5A1A2Q1. When the output frequency of master oscillator A1 is below its geometric mean of 355 MHz, the command voltage is 0 volts and switches A5A1A2Q1 and A5A1A2Q2 are both in cutoff. Switch A5A1A2Q3, however, is saturated due to its base being tied to +6 volts through reed relays A5A1K1 and A5A1K2, resistor A5A1A2R3 and diode A5A1A2CR3, energizing reed relays A5A1K3 and A5A1K4 to insert the appropriate low end low-pass filter into the signal path. Note that resistor A5A1A2R3 limits the current flow through relays A5A1K1 and A5A1K2 to a level below that value which is required for energization of the relays. Each low end filter has an extremely sharp skirt at its high frequency limit to sharply attenuate harmonics of the carrier frequency generated either by the frequency divider, modulator or power amplifier.

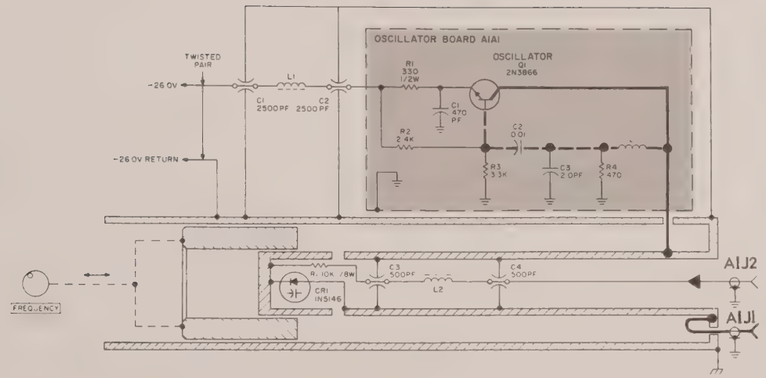
4-72. Similarly, when the output frequency of master oscillator A1 is above its geometric mean of 355 MHz, the band center command voltage obtained from the frequency counter is +5 volts. This level drives both A5A1A2Q1 and A5A1A2Q2 into saturation, energizing reed relays A5A1K1 and A5A1K2 to insert the appropriate high end low-pass filter into the signal path. Note that saturation of A5A1A2Q2 cuts off A5A1A2Q3 and prevents energization of relays A5A1K3 and A5A1K4. Each high end filter, like each low end filter, has an extremely sharp skirt at its high frequency limit to greatly attenuate unwanted harmonics of the carrier frequency.

4-73. The output of the selected low-pass filter (as determined by the setting of the RANGE MHz switch and the operating frequency of the master oscillator) is simultaneously applied to the RF level detector of the balanced modulator and level control circuitry; and, through an R-C network (A5A1A1R2, A5A1A1C1 and A5A1A1C2) that establishes the 50-ohm source impedance, to the 0-150 dB attenuator circuitry.

4-74. When the RANGE MHz switch is set to PLUG-IN, a magnet on the rotor of the turret switch is placed in close proximity to reed relay A5A1A1K6. Closure of the relay contacts energizes reed relay A5A1K5, coupling the output of the plug-in frequency extender module to both the RF level detector and the output attenuator. Note that diodes A5A1A2CR1 and A5A1A2CR2 clamp the bases of A5A1A2Q1 and A5A1A2Q3 respectively, at ground. The output of the plug-in module is coupled through A5A1A1R3 (which establishes the plug-in module output impedance at 50 ohms) to both the output attenuator and, via A5A1A1R2, A5A1A1C1 and A5A1A1C2, to the RF level detector.

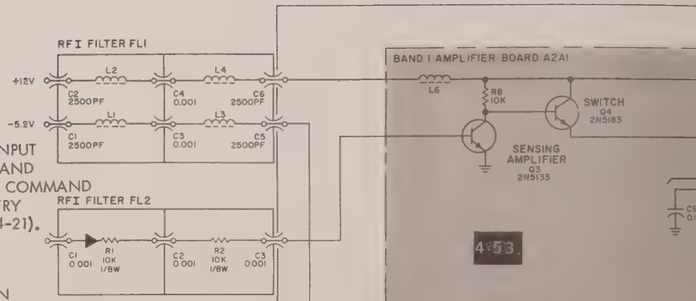


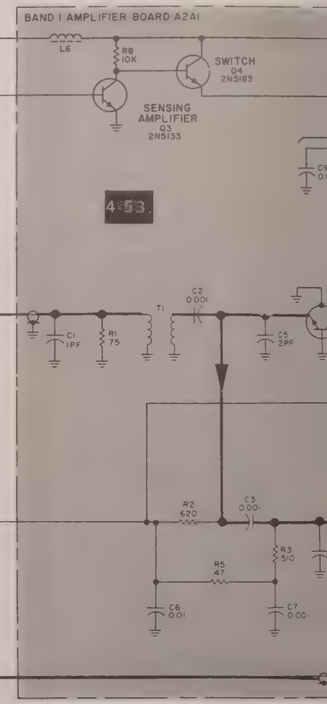
A2
Parts Locations



FM DEVN/VERNIER/AFC VOLTAGE FROM MODULATION SELECTION & AM/FM METERING CIRCUITRY (FIGURE 4-20).

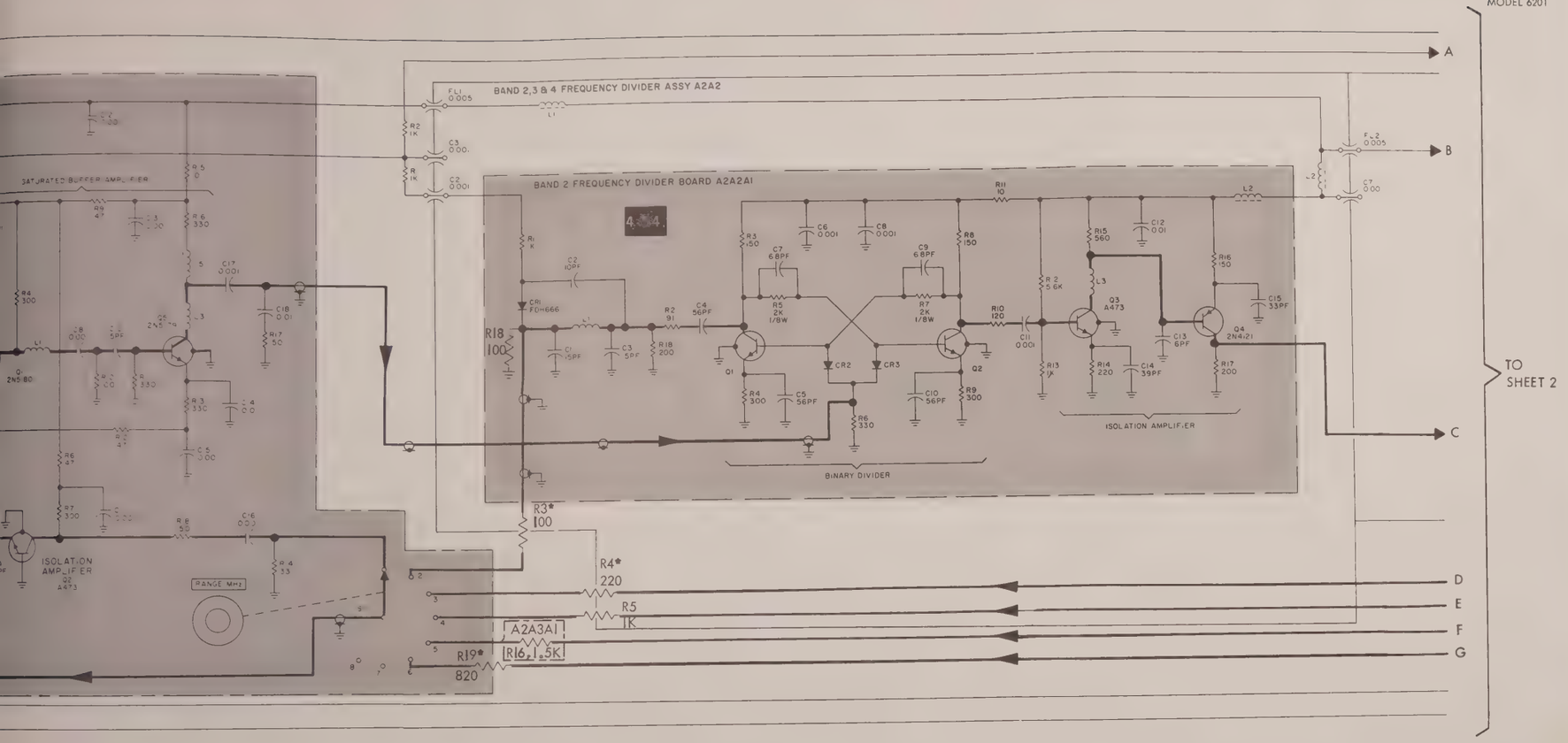
LEVEL INPUT FROM BAND CENTER COMMAND CIRCUITRY (FIGURE 4-21).





NOTES
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 WATT
2. ALL CAPACITOR VALUES ARE IN MICROFARADS
3. [RANGE MHz] SWITCH SHOWN IN [248-512] POSITION
4. * INDICATES FACTORY SELECT COMPONENT NOMINAL VALUE SHOWN

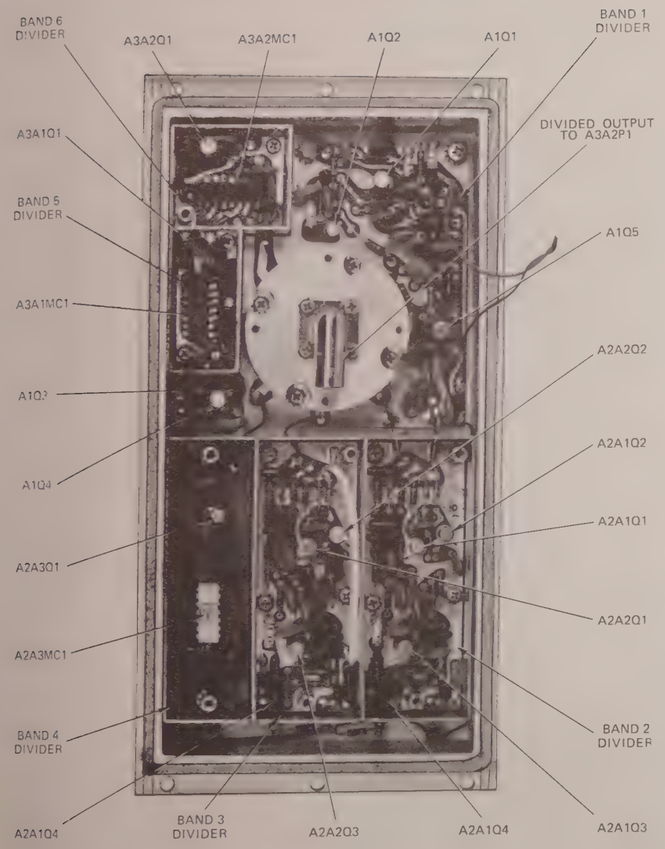
7.75 MHz TO 512 MHz OUTPUT TO BALANCED MODULATOR & LEVEL CONTROL CIRCUITRY (Fig. 4-16)



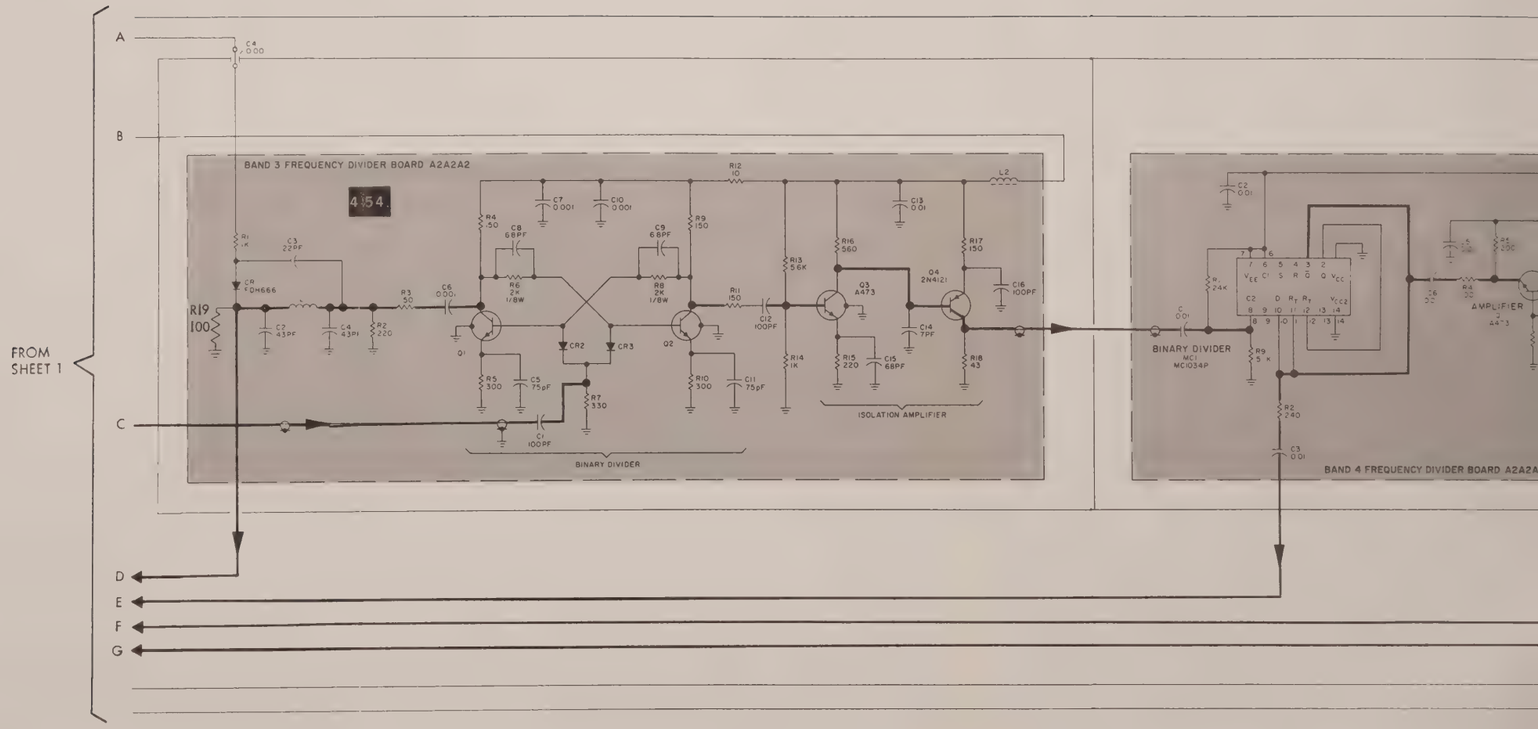
A1/A2

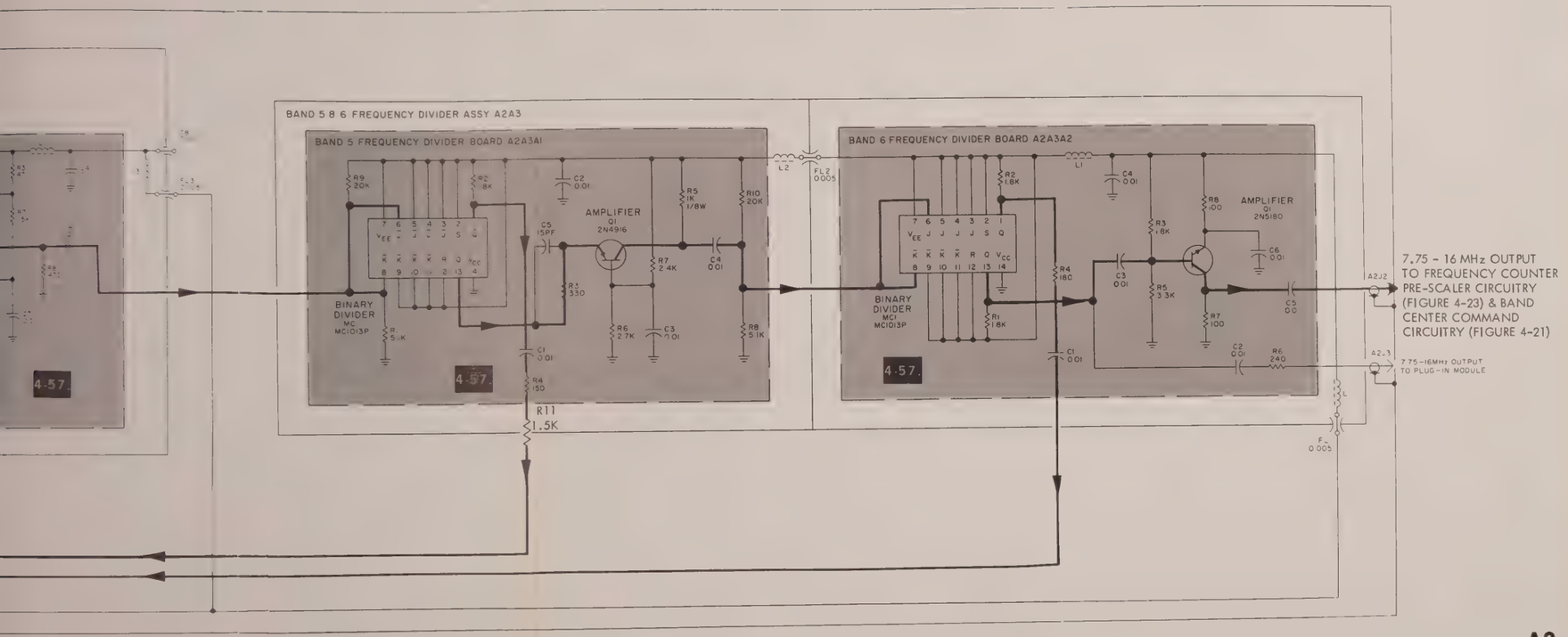
4-15.

Figure 4-15. Frequency Generation Circuitry, Functional Schematic Diagram (Sheet 1 of 2)



A2
Parts Locations

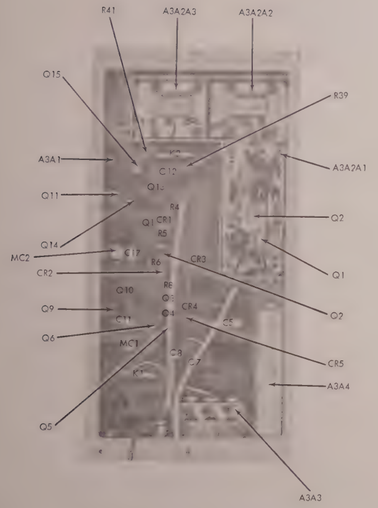




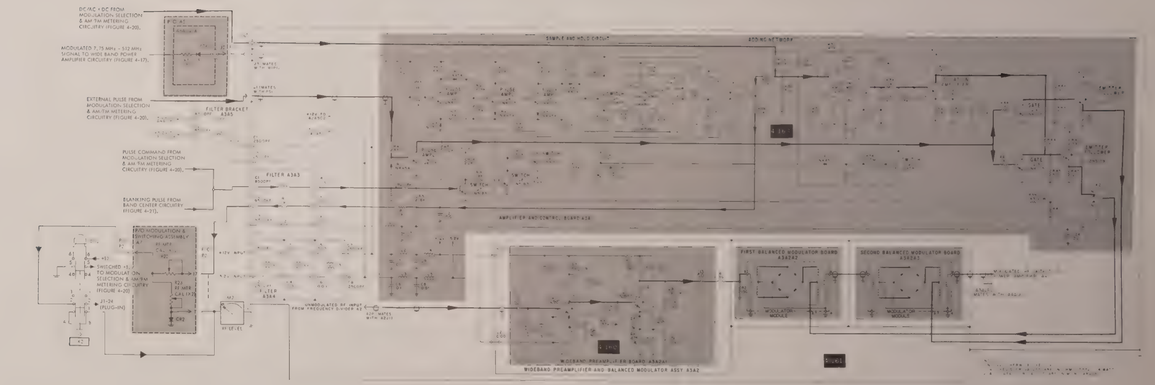
A2

4 - 15.

Figure 4-15. Frequency Generation Circuitry, Functional Schematic Diagram (Sheet 2 of 2)

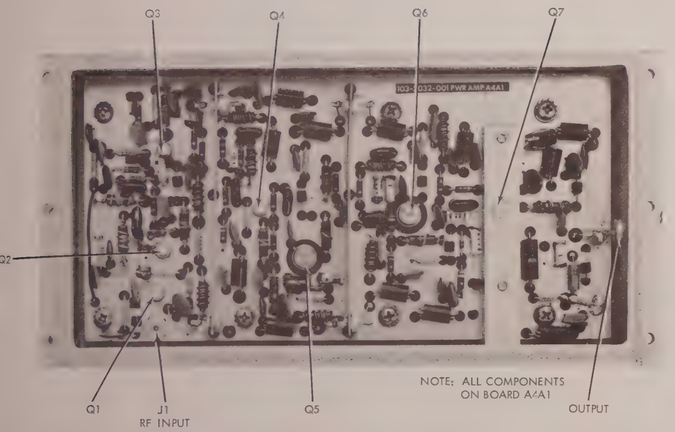


A3
Parts Locations

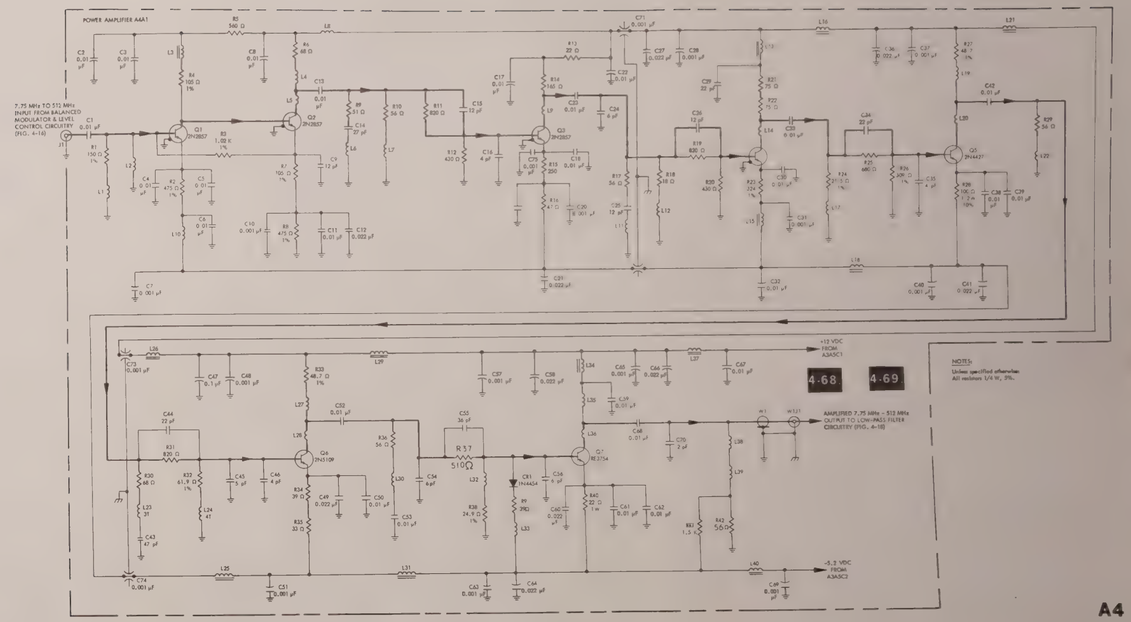


A3
4 - 16.

Figure 4-16. Balanced Modulator and Level Control Circuitry, Functional Schematic Diagram



A4
Parts Locations



A4
4-17.

Figure 4-17. Wideband Power Amplifier Circuitry, Functional Schematic Diagram

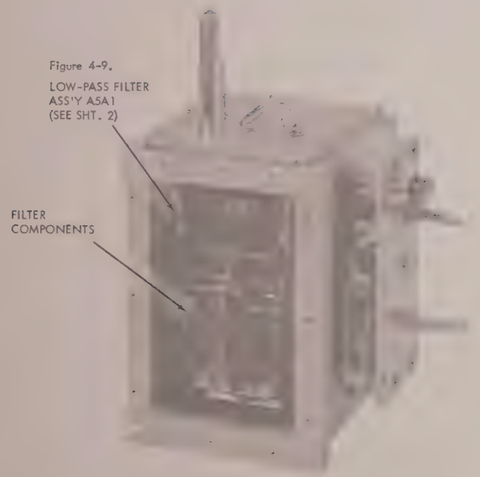
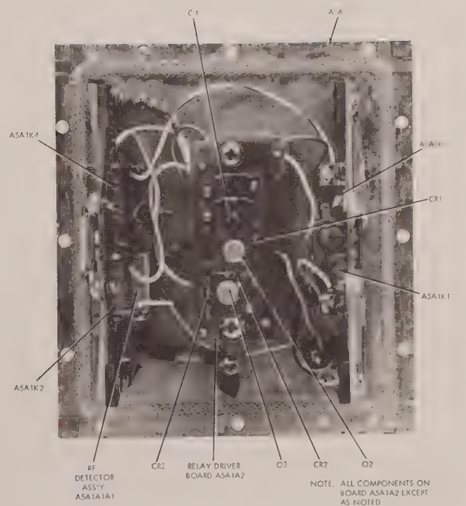
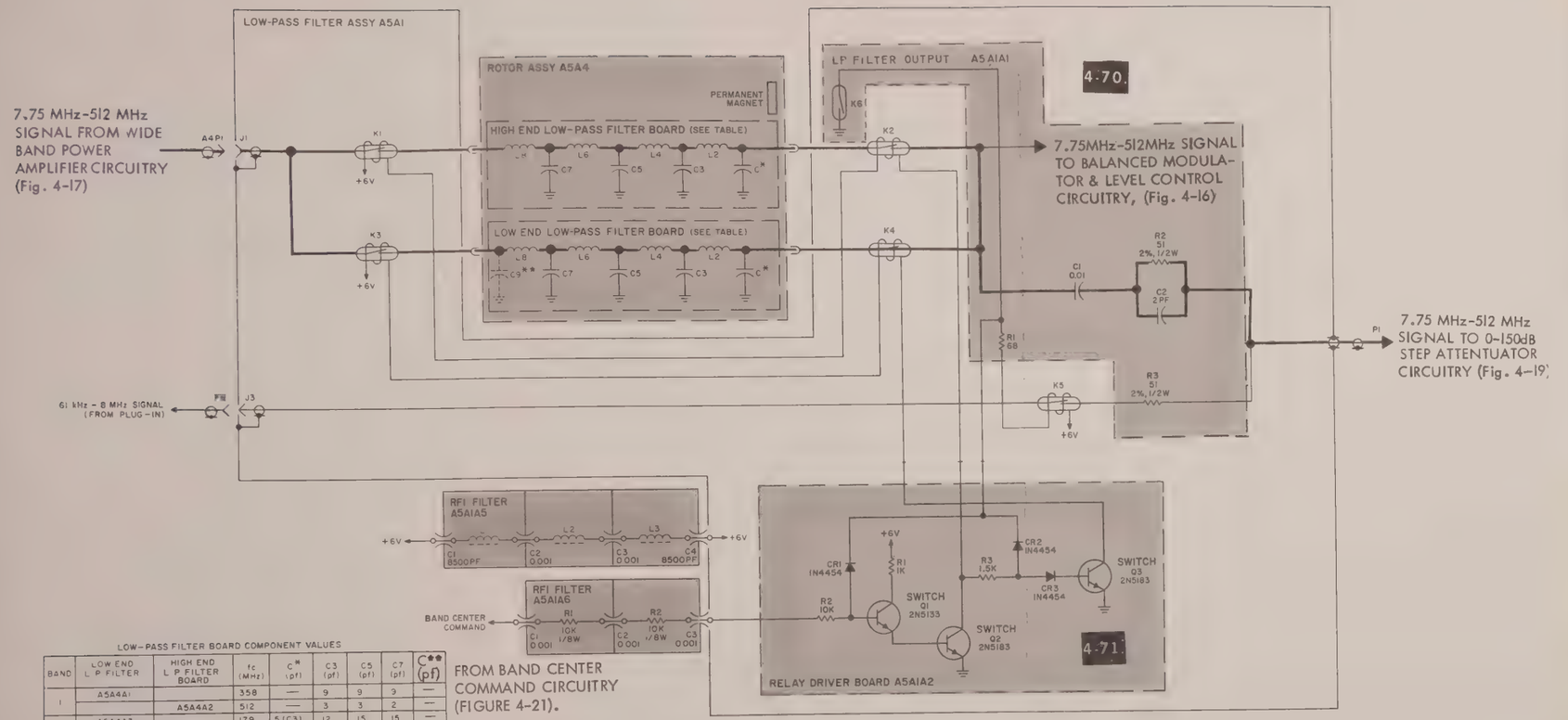


Figure 4-9.
LOW-PASS FILTER
ASS'Y A5A1
(SEE SHT. 2)





LOW-PASS FILTER BOARD COMPONENT VALUES

BAND	LOW END L P FILTER	HIGH END L P FILTER BOARD	fc (MHz)	C* (pf)	C3 (pf)	C5 (pf)	C7 (pf)	C** (pf)
1	A5A4A1		358	—	9	9	3	—
		A5A4A2	512	—	3	3	2	—
2	A5A4A3		179	5 (C3)	12	15	15	—
		A5A4A4	256		10	10	8	—
3	A5A4A5		89.5	20 (C5)	33	30	27	—
		A5A4A6	128	15 (C4)	24	22	18	—
4	A5A4A7		44.75	43 (C7)	68	62	51	—
		A5A4A8	64	30 (C6)	47	43	36	—
5	A5A4A9		22.37	82 (C9)	130	130	100	—
		A5A4A10	32	56 (C8)	91	91	75	—
6	A5A4A11		11.187	160 (C11)	270	240	200	30 (C12)
		A5A4A12	16	120 (C10)	180	180	150	—

NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS, ± 5%, 1/4 WATT
2. ALL CAPACITOR VALUES ARE IN MICROFARADS
** PARTS OF ROTOR ASSEMBLY A5A4
* C9 4 pF A5A4A4

A5

4 -18.

Figure 4-18. Low Pass Filter Circuitry, Functional Schematic Diagram

4-75. 0 - 150 dB STEP ATTENUATOR CIRCUITRY. Figure 4-19.

4-76. The RF output level of the signal from the low-pass filter circuitry is adjustable over a 16 dB range with dBm continuous control A6A1R1. To provide continuous adjustment of the RF level over a 166 dB range, the 70 dB attenuator control assembly (A6A2) and the 80 dB attenuator control assembly (A6A1) are employed. Assembly A6A2 consists of 10 dB, 20 dB, and 40 dB chip (two 20 dB chips in series) attenuators, which provide up to 70 dB of attenuation, in 10 dB steps. In this attenuator control assembly lamps A6A2A2DS1 through DS3 control the operation of electronic switches A6A2A1Q1 through Q9, via phototransistors A6A2A1PT1 through PT3. Assembly A6A1 consists of four 20 dB chips, a total of 80 dB which is inserted in one step. In this attenuator control assembly, lamp A6A1A1DS1 controls the operation of electronic switches A6A1A2Q1 through Q6, via phototransistor A6A1A2PT1. The desired attenuation, from 0 to 150 dB, is obtained by inserting and bypassing various combinations of the 10, 20 40 and 80 dB attenuators as indicated in Table 3-1 and described in paragraph 3-37.

4-77. MODULATION SELECTION AND AM/FM METERING CIRCUITRY. Figure 4-20.

4-78. RF Level Set Network. This resistive network consisting of A7R1, A7R3, A7R5 and A6A1R1 provides a DC level output which represents the average power of the RF output. During AM operation, an AC signal is added to this DC level. The level set network operates as follows. When in CW, FM or pulsed operation, resistor A7R5 is returned to ground through the released AM INT and AM EXT pushbuttons. With the VX2 pushbutton in the released position, the +12 volts DC applied to A7R3 results in approximately a +4 volts output from the RF level set network is applied to the balanced modulator and level control circuitry (paragraph 4-59). When the VX2 pushbutton is pressed, switched +12 volts is applied to the junction of A7R1 and A7R3, effectively shorting output A7R3. This results in a 0 to +8 volts output from the RF level set network. During AM operation, the AC signal developed across the AM LEVEL control is added to the DC level at the junction of A7R5 and A7R6. Factory-selected resistor A7R7 places the summing point at DC ground.

4-79. 1 kHz Oscillator. The following subparagraphs describe the stages of the 1 kHz oscillator.

4-80. AGC Amplifier A7A1. This stage is an inverting IC operational amplifier which is disabled by the negative DC voltage at its inverting terminal (pin 2), when the AM INT and FM INT pushbuttons are both in the released position. Under this condition, a positive DC output is obtained from the amplifier. When either the AM INT or FM INT pushbutton is pressed, +12 volts is applied to the junction of A7R85 and A7R24. The resulting positive DC voltage at the inverting terminal of the amplifier enables it. Under this condition, a negative DC output is obtained from the AGC amplifier.

4-81. FET A7Q2. This P-channel FET is normally held at cutoff by the positive DC output of the AGC amplifier. When the AM INT or FM INT pushbutton is pressed, the negative DC output of the AGC amplifier gates the FET on. The FET then acts as a variable resistor under the control of the applied negative DC signal from A7A1.

4-82. Oscillator A7A2 and Filter A7A3. Stage A7A2 employs an IC operational amplifier in a Wien bridge oscillator configuration. With FET A7Q2 at cutoff, the feedback network at the inverting terminal (pin 2) of A7A2 is principally composed of A7R35 and A7R32. Under this condition, the oscillator is disabled. When the FET is gated on, A7C8 and the FET are bridged across A7R32, causing the oscillator to be enabled. Rear panel INT MOD ADJ screwdriver control R3 varies the resistance of the R-C phase shifting network at the non-inverting terminal (pin 3) of A7A2, thus varying the oscillator frequency ±2 percent of 1 kHz. The oscillator output is coupled through active IC filter network A2A3 to the front panel MOD OUT 1 kHz connector and the AM LEVEL or FM DEV control. Any variation in the oscillator output is sensed by peak detector A7CR5 and A7C7, and applied to the non-inverting terminal (pin 3) of AGC amplifier A7A1. The resulting output of A7A1 then controls the resistance of the FET in such a manner as to return the output level of the 1 kHz oscillator to the proper value (2.0 volts peak-to-peak, nominal).

4-83. FM Amplifier. This stage consists of difference amplifier A7Q3/Q4 and output amplifier A7Q6. When in internal or external FM operation, the FM input is coupled through A7Q3A to the base of A7Q4A. At this time, the vernier/AFC output of the frequency lock circuitry (paragraph 4-127) is coupled through A7Q3B to the base of A7Q4B. The resulting output at the collector of A7Q4B is routed through output amplifier A7Q6 to the master oscillator varactor (via the pressed FM INT or FM EXT pushbutton).

4-84. AM Metering Circuit. This circuit comprises a buffer amplifier and an AC detector. Stage A7Q1, a common-emitter amplifier, isolates the succeeding AC detector from the internal 1 kHz oscillator and external AM circuits. Diode A7CR1 and capacitor A7C5 provide peak detection of the AM signal. The peak detected output is routed through resistor A7R13 and % AM cal potentiometer A7R14 to the % AM/FM DEV meter, when the AM/FM switch is set to AM.

4-85. FM Metering Circuit. The following subparagraphs describe the stages of the FM metering circuit.

4-86. FM Metering Buffer A7A4. This stage is a non-inverting IC operational amplifier (with a gain of approximately 6) which provides isolation for the FM peak deviation metering outputs.

4-87. Range Buffer A7A3. This stage is a non-inverting IC operational amplifier (with a gain of approximately 80) which isolates the meter multipler networks (A7R15-R21; and A7S7-S10) from the succeeding AC detector.

4-88. AC Detector A7A6. This stage is a non-inverting IC operational amplifier which peak detects the negative alternation of the applied AC signal. Diode A7CR10 and capacitor A7C35 provide peak detection of the signal. The feedback loop to the inverting input terminal of A7A6 is closed by A7CR9 for the positive alternation of the AC signal,

thereby preventing damage to A7A6. Similarly, the feedback loop to the non-inverting input terminal is closed by the diode detector and the succeeding DC amplifier stage for the negative alternation of the AC signal.

4-89. DC Amplifier A7A7. This stage is an inverting IC operational amplifier which amplifies the peak detected output of A7A6 sufficiently to obtain full-scale calibrated readings on the % AM/FM DEV meter for the 30-, 100-, 300- and 1000-kHz FM peak deviation ranges provided by the FM RANGE (kHz) pushbuttons. Potentiometer A7R72 provides electrical zeroing for the FM deviation scales of the % AM/FM DEV meter. FM dev meter cal potentiometer A7R77 provides an adjustment for the 100 kHz FM peak deviation metering output.

4-90. BAND CENTER COMMAND CIRCUITRY. Figure 4-21.

4-91. Amplifier/Limiter A8A3A6Q6 and A8A3A6Q5. This circuit is a two-stage capacitor-coupled amplifier. Each stage is a common-emitter amplifier. Diodes A8A3A6CR4 and CR2 limit the positive and negative swings of the 7.75 to 16 MHz signal applied to the succeeding low-pass filter.

4-92. Low-pass Filter. This circuit is L-type filter consisting of capacitor A8A3A6C3 and inductor A8A3A6L1. The characteristics of the low-pass filter are such that its insertion loss is approximately 5 dB at 11.093 MHz, which corresponds to the geometric mean (355 MHz) of the master oscillator tuning range.

4-93. Detector. Diode A8A3A6CR1 and the R-C network composed of capacitor A8A3A6C2 and resistor A8A3A6R6 peak detect the negative alternation of the low-pass filter output signal. Potentiometer A8A3A6R2 adjusts the DC bias level on which the detector output rides.

4-94. Schmitt Trigger A8A3A6Q1 and A8A3A6Q2. When the signal applied to the low-pass filter is below the geometric mean of the master oscillator tuning range, the negative output of detector A8A3A6CR1 causes A8A3A6Q1 to be turned off and A8A3A6Q2 to be turned on. Under this condition, the output of A8A3A6Q2 is approximately +2 volts DC. When the signal applied to the low-pass filter is at or above the geometric mean, the detector output goes positive (by virtue of the 5 dB insertion loss of the low-pass filter and the positive DC voltage from A8A3A6R2), thereby causing the Schmitt trigger to change state. Under this condition, the output of A8A3A6Q2 is +5 volts DC. Potentiometer A8A3A6R1 adjusts the hysteresis of the Schmitt trigger so that triggering occurs at 11.10 MHz when tuning up in frequency and 10.90 MHz when tuning down.

4-95. Gates A8A3A6Q3 and A8A3A6Q4. These gates convert the Schmitt trigger outputs to the TTL logic levels required by the succeeding delay logic circuit. The output of gate A8A3A6Q4 is a logical ZERO level (0 volts DC nominal) for frequencies below the geometric mean and a logical ONE level (+5 volts DC nominal) for frequencies equal to or above the mean.

4-96. Delay Logic Circuit. This circuit comprises monolithic, TTL, inverters in A8A3A6IC1 and two-input AND/OR invert gates in A8A3A6IC2. The output of gate A8A3A6Q4 is coupled through two inverters in IC1 to provide the band center command level (see Figure 4-22). The gate A8A3A6Q4 output is also applied to the remainder of the delay logic circuit, which provides a trigger pulse of approximately 2.25 microseconds to the output monostable multivibrator (one-shot). The R-C network composed of A8A3A6R17 and A8A3A6C9 determines the pulse width of the trigger pulse.

4-97. Monostable Multivibrator A8A3A6IC3. This monolithic TTL one-shot provides a positive output pulse which blanks the RF output (via the balanced modulator and level control circuitry) for the time required to switch low-pass filters in assemblies A2 and A5. Capacitor A8A3A6C7 and an internal timing resistor (2 kilohms nominal) in A8A3A6IC3 set the output pulse width at approximately10 milliseconds.

4-98. FREQUENCY COUNTER PRE-SCALER CIRCUITRY. Figure 4-23.

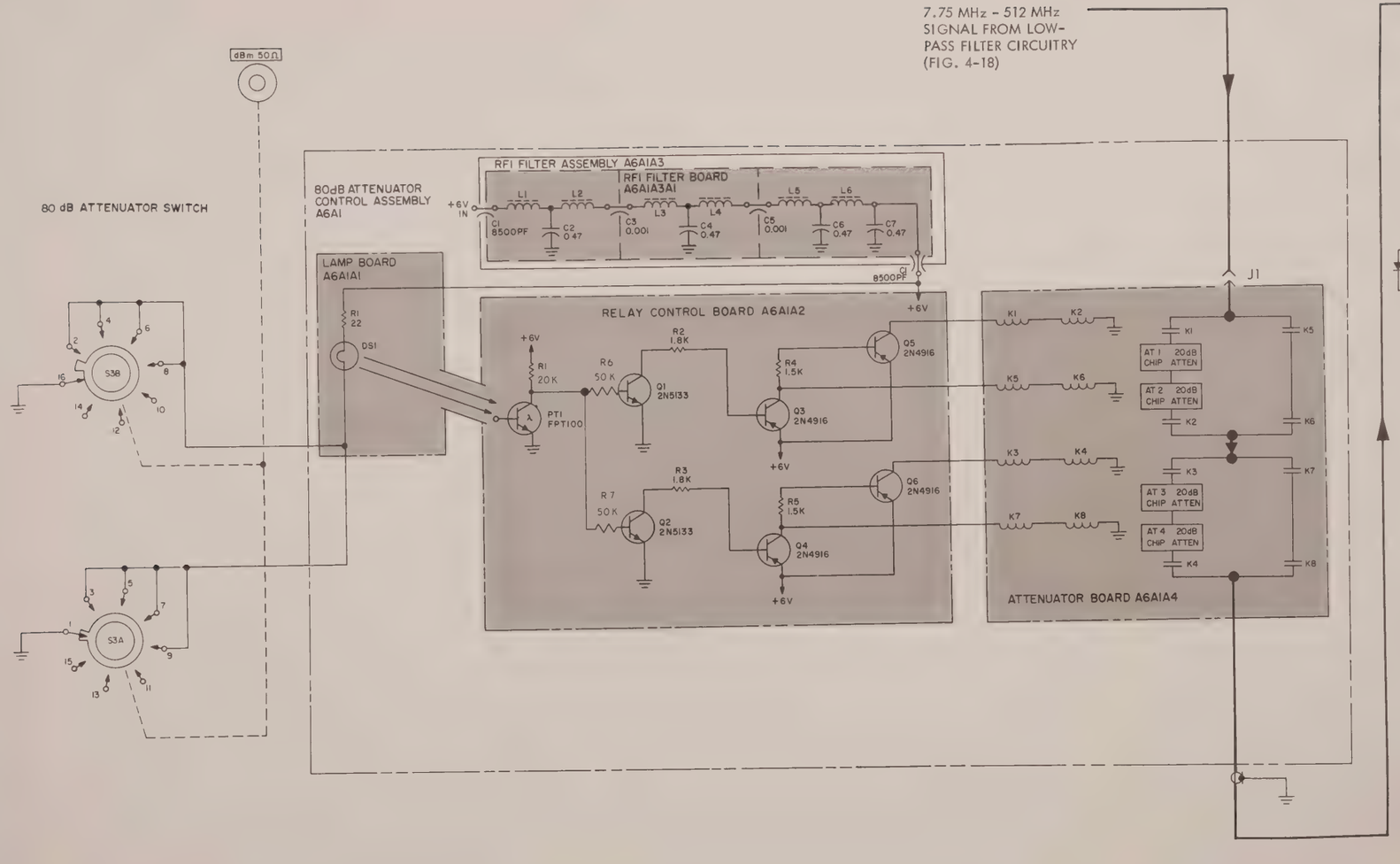
4-99. Amplifier A8A3A4Q1. This stage is a capacitor-coupled, common-emitter amplifier. Diode A8A3A4CR1 amplitude limits the negative alternation of the applied 7.75 to 16 MHz squarewave signal from the frequency generation circuitry (refer to paragraph 4-50).

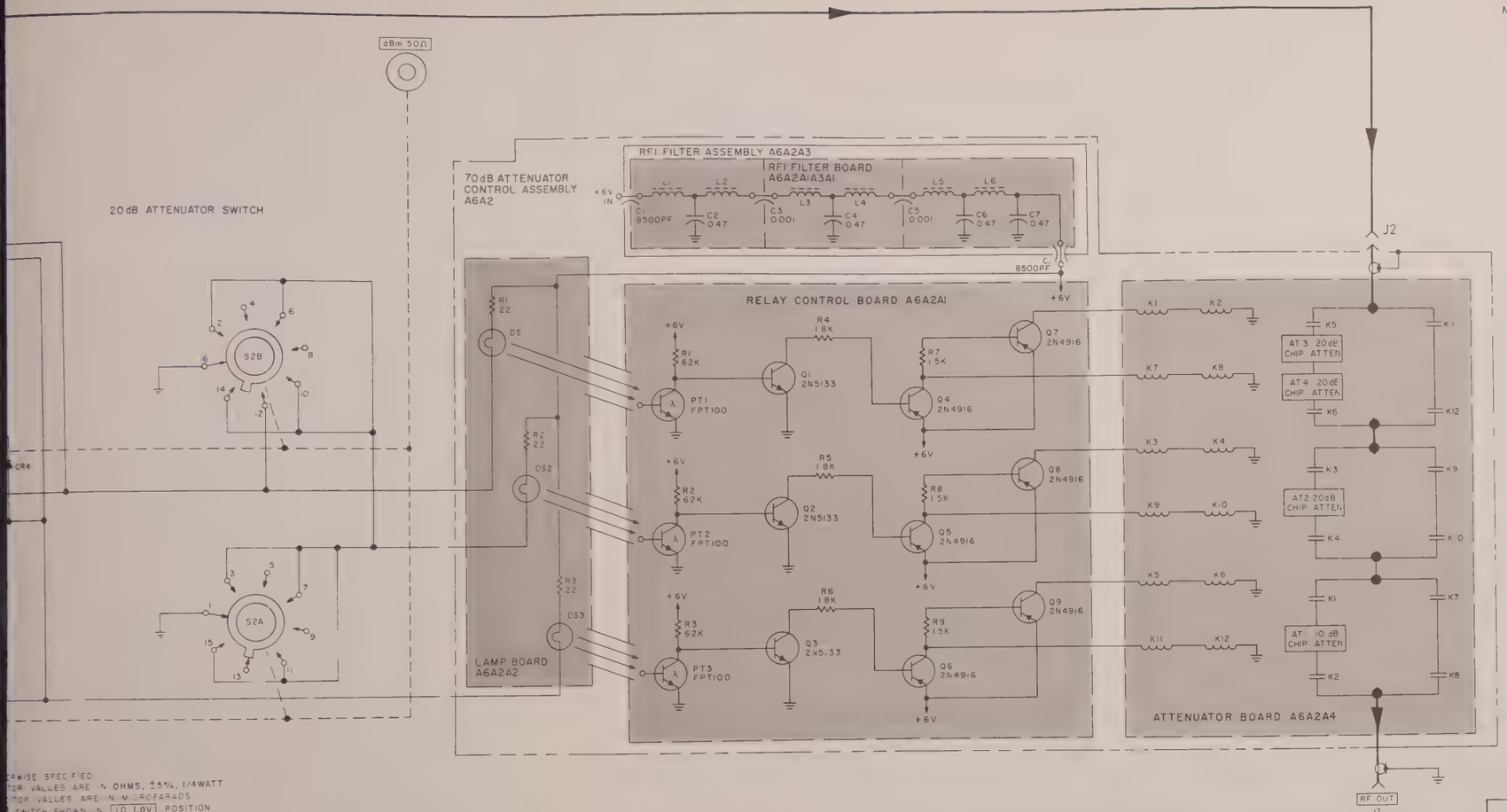
4-100. Frequency Divider A8A3A4IC1-IC3. This circuit comprises three monolithic, TTL, D-type flip-flops in cascade. Each of these edge-triggered flip-flops functions as a binary divider. During external count operation, the internal/external selector logic applies a logical ZERO level to the clear input of the first flip-flop. This input disables the frequency divider.

4-101. Emitter Follower A8A3A4Q2, Amplifier A8A3A4Q3, and Emitter Follower A8A3A4Q4. Stage A8A3A4Q2 provides a low impedance path to amplifier A8A3A4Q3. This emitter follower also isolates external circuits (which are coupled to the EXT COUNT connector) from succeeding circuits. Amplifier A8A3A4Q3 is a capacitor-coupled, common-emitter amplifier. Diode A8A3A4CR2 amplitude limits the negative alternation of the external count signal. Emitter follower A8A3A4Q4 isolates the amplifier from the succeeding TTL logic circuits.

4-102. Pulse Shaper. This Schmitt trigger employs two of the monolithic, TTL inverters in A8A3A4IC5. The resulting 0V to +5V squarewave output of the pulse shaper is applied to the internal/external count selector logic.

4-103. Pre-scaled Frequency Selector Logic. This logic comprises the following monolithic, TTL gates in A8A3A4IC7: four, dual-input AND gates and an OR invert gate. One of three frequency divider outputs ($F_o/8$, $F_o/16$, or $F_o/32$) or the external count signal is selected by the pre-scaled frequency


7.75 MHz - 512 MHz
SIGNAL FROM LOW-
PASS FILTER CIRCUITRY
(FIG. 4-18)
dBm 50Ω
80 dB ATTENUATOR SWITCH
80dB ATTENUATOR
CONTROL ASSEMBLY
A6AI
RFI FILTER ASSEMBLY A6AIA3
RFI FILTER BOARD
A6AIA3AI
+6V
IN
L1
L2
L3
L4
L5
L6
C1
8500PF
C2
0.47
C3
0.001
C4
0.47
C5
0.001
C6
0.47
C7
0.47
C1
8500PF
LAMP BOARD
A6AIAI
R1
22
DS1
RELAY CONTROL BOARD A6AIA2
+6V
R1
20K
PT1
FPT100
R6
50K
R2
1.8K
Q1
2N5133
R4
1.5K
Q3
2N4916
Q5
2N4916
R7
50K
R3
1.8K
Q2
2N5133
R5
1.5K
Q4
2N4916
Q6
2N4916
J1
K1
K2
K3
K4
K5
K6
K7
K8
AT 1 20dB
CHIP ATTEN
AT 2 20dB
CHIP ATTEN
AT 3 20dB
CHIP ATTEN
AT 4 20dB
CHIP ATTEN
ATTENUATOR BOARD A6AIA4
S3B
S3A
10 & 40dB ATTENUATOR SWITCH
CR5
CR6
CR8
CR7
CR1
CR2
CR3
S1B
S1A
4-75.
4-76.

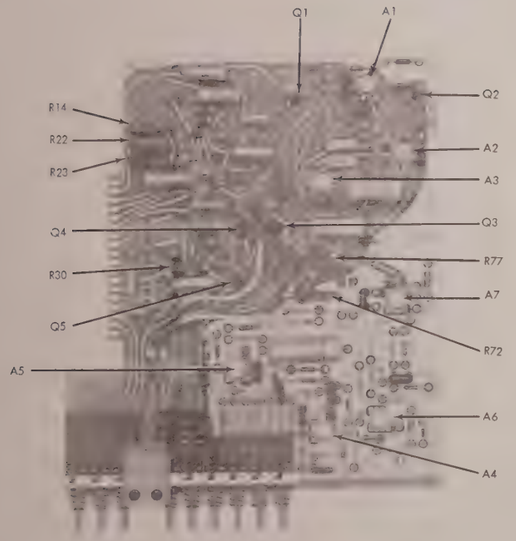


ERWISE SPECIFIED
OR VALUES ARE IN OHMS, ±5%, 1/4WATT
TOR VALUES ARE IN MICROFARADS
SWITCH SHOWN IN 10 1.0V POSITION
W FRONT PANEL END OF SHAFT
ARE TYPE 1N4454

A6

4-19.

Figure 4-19. 0-150 dB Step Attenuator Circuitry, Functional Schematic Diagram



A7
Parts Locations

MODULATION & SWITCHING ASSEMBLY A7

AFC VERNIER VOLTAGE FROM FREQUENCY LOCK CIRCUITRY (FIGURE 4-32)

FM J12

1 kHz OSCILLATOR

4-79

SWITCHED +12V

A1 LM101A

A2 LM101A

A3 LM101A

Q2 2N5460

CR12 1N4742A

DS1

S1 AM PULSE

S2 AM EXT

S3 AM INT

S4 CW

S5 FM INT

S6 FM EXT

TO S3

FROM CW LAMP DS1

FM CAL VOLTS ADJ

FM DEV

FM DEVN VERNIER AFC VOLTAGE TO FREQUENCY GENERATION CIRCUITRY (FIGURE 4-15)

MOD OUT 1 kHz J11

EXT PULSE INPUT

PULSE CMD (SWITCHED +12V)

AM LEVEL

TO BALANCED MODULATOR & LEVEL CONTROL CIRCUITRY (FIGURE 4-16)

SWITCHED +12V FROM VX2 PUL FROM VX2 PUSHBUTTON (FIGURE 4-16)

AM PULSE J10

-76V

-5.2V

+12V

GND

** FACTORY-SELECTED; INSTALLED TEST
* FACTORY-SELECTED; NOMINAL VALUE SHOWN
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 1%
1. ALL CAPACITOR VALUES ARE IN MICROFARADS

NOTES, UNLESS OTHERWISE SPECIFIED:

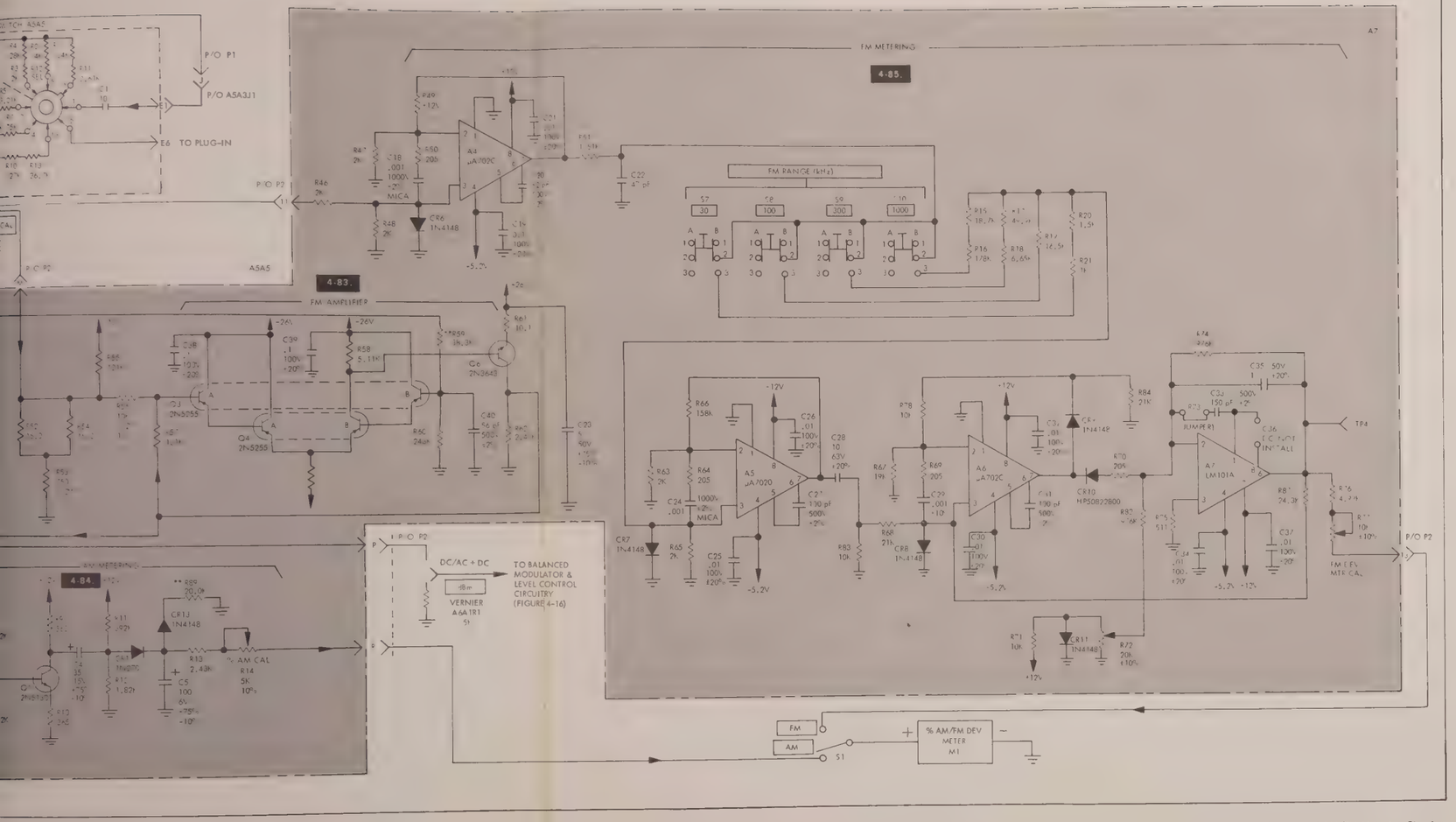
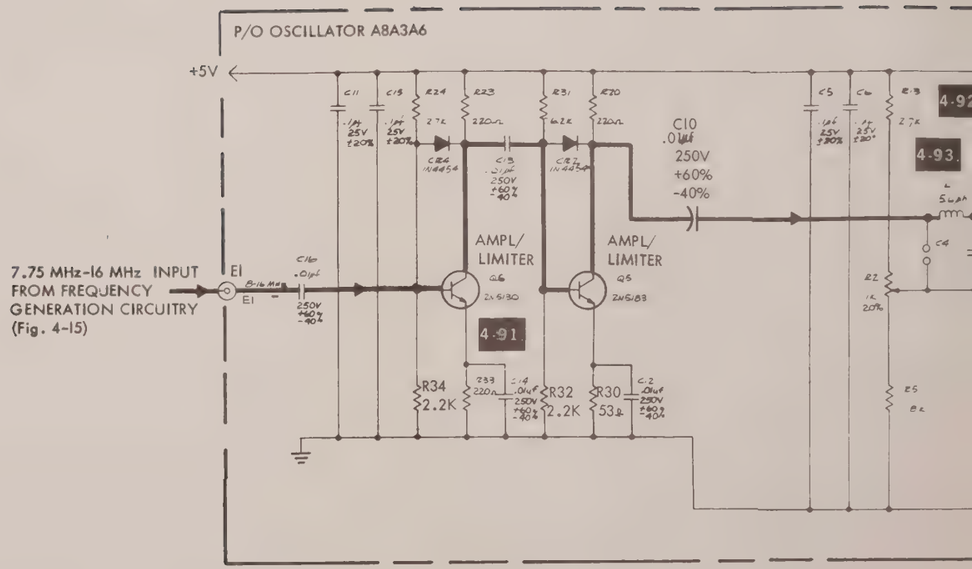


Figure 4-20. Modulation Selection and AM/FM Metering Circuitry

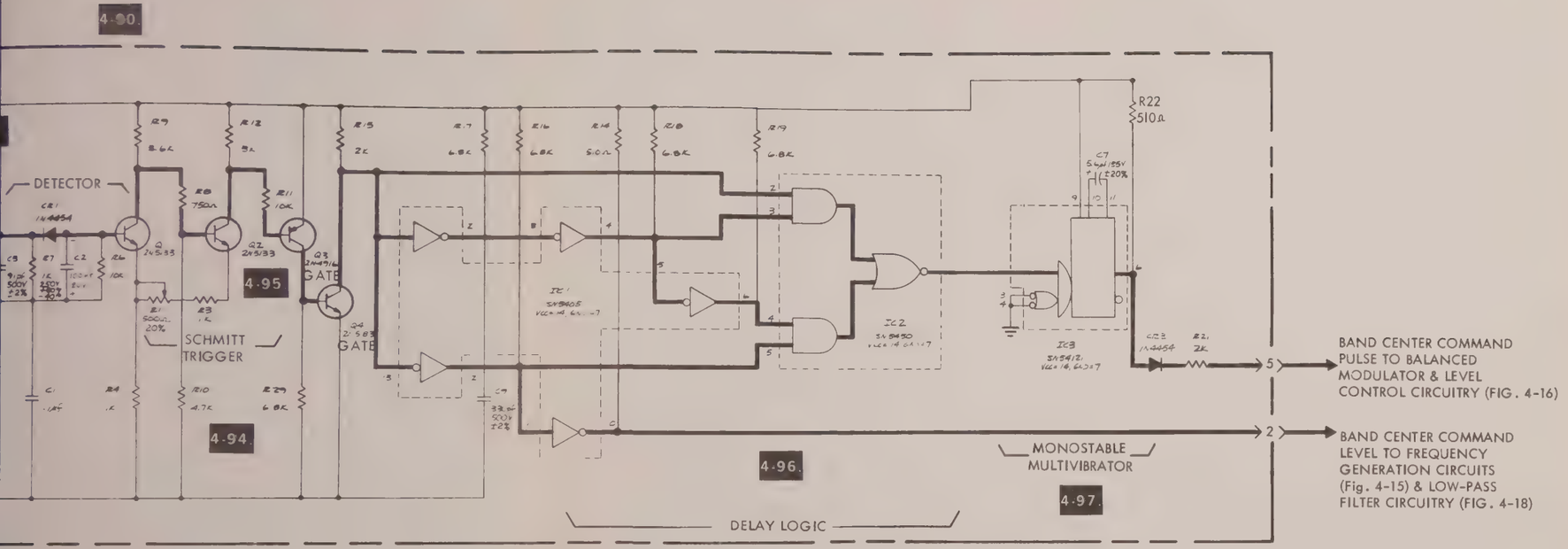
A8 A3 A6
Parts Locations



NOTES: (UNLESS SPECIFIED OTHERWISE)

1. ALL RESISTORS 1/4 W, 5% CARBON.

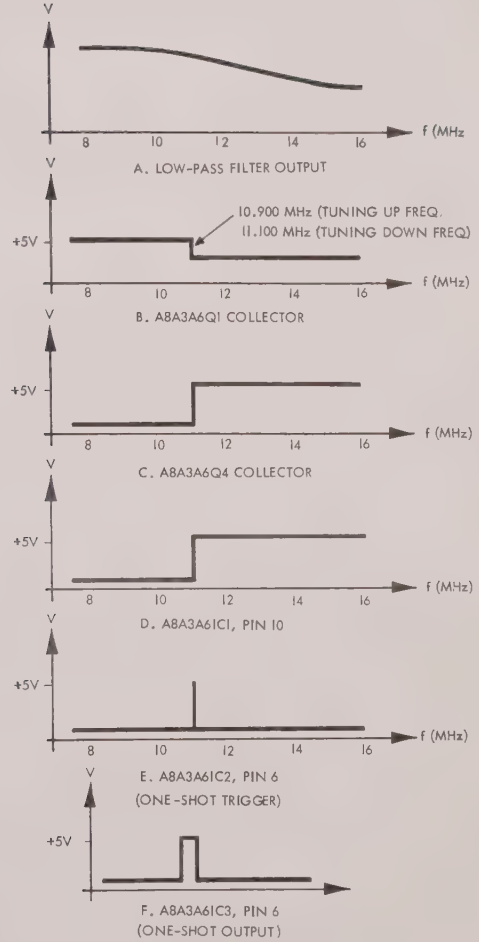
*FACT. SELECT, NOMINAL VALUE SHOWN



A8/A3/A6

4-21.

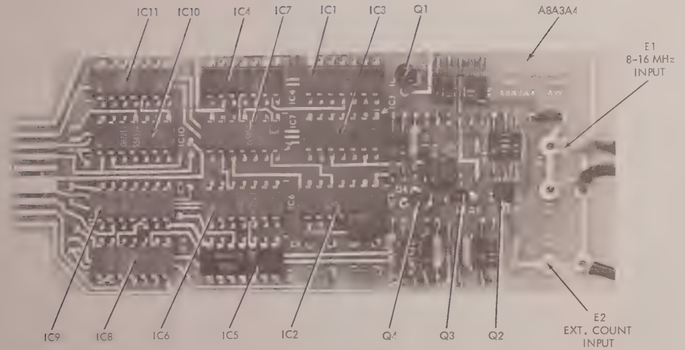
Figure 4-21. Band Center Command Circuitry, Functional Schematic Diagram



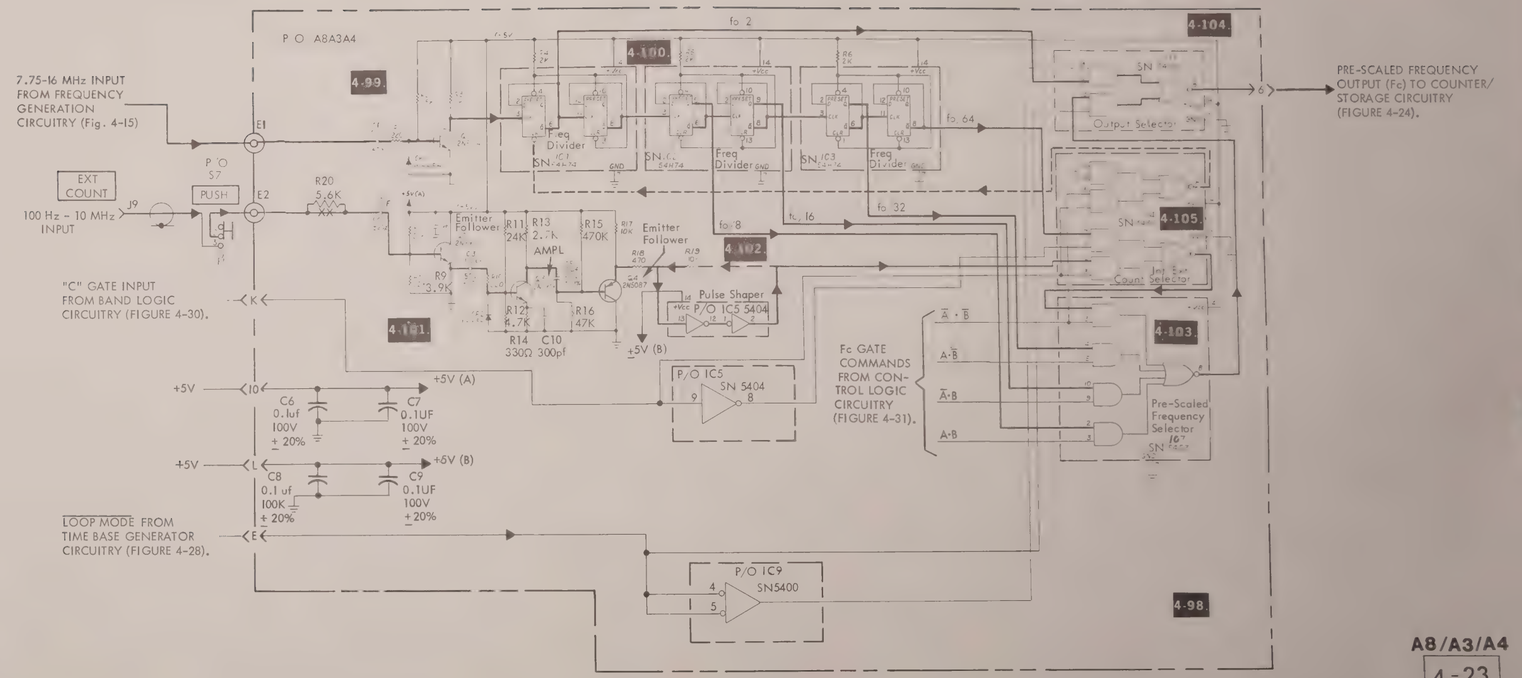
A8

4-22.

Figure 4-22. Band Center Command Waveforms



A8 A3 A4
Parts Locations



A8/A3/A4
4 - 23.

Figure 4-23. Frequency Counter Pre-Scaler Circuitry, Functional Schematic Diagram

selector logic, when the corresponding F_c gate command ($\overline{A} \cdot \overline{B}$, $A \cdot \overline{B}$, $\overline{A} \cdot B$, or $A \cdot B$) from the control logic circuitry (paragraph 4-125) is a logical ONE level. Table 4-10 indicates the count frequency (F_c) selected by the pre-scaled frequency selector logic during the internal and external count modes. (Note that the $F_o/64$ divider output is not included. This output is only employed for the lowest frequency band generated by the plug-in module.)

4-104. Output Selector Logic. This logic in A8A3A4IC11 is identical to the pre-scaled frequency selector logic, except only two, dual-input AND gates are provided. Either the $F_o/2$ output of the frequency divider or the pre-scaled frequency selector logic output is selected by the output selector logic, when the LOOP MODE input from the time base generator circuitry (paragraph 4-117) is a logical ZERO level or ONE level, respectively. An inverter in A8A3A4IC9 applies a logical ONE level to the AND gate associated with the $F_o/2$ signal, when the LOOP MODE input is a logical ZERO level.

4-105. Internal/External Count Selector. This logic in A8A3A4IC4 is identical to the output selector logic, except an additional gate and an OR invert gate are provided to generate the frequency divider disable signal. Either the $F_o/64$ output of the frequency divider or the shaped external count signal is selected by the internal/external count selector logic, when the "C" gate input from the band logic circuitry (paragraph 4-123) is a logical ZERO level or ONE level, respectively. An inverter in A8A3A4IC5 applies a logical ONE level to the AND gate associated with the $F_o/64$ signal, when the "C" gate input is a logical ZERO level. When operating in the external count mode, the "C" gate input and the $\overline{A} \cdot \overline{B}$ gate command are both a logical ONE level. This results in a logical ZERO level output from the additional OR invert gate in A8A3A4IC4, thereby disabling the frequency divider during external count operation.

4-106. FREQUENCY COUNTER, COUNTER/STORAGE CIRCUITRY. Figure 4-24.

4-107. Count Input Logic. This logic consists of three, dual-input positive NAND gates in A8A3A3IC13. During normal count operation, the UPGATE (ΔT) and DOWNGATE commands from the time base generator circuitry (paragraph 4-117) are a logical ONE level and ZERO level, respectively. This results in the F_c pulses from the pre-scaler circuitry (paragraph 4-98) being applied to the count up input (pin 5) of up/down decade counter A8A3A3IC1 for the duration of the UPGATE command. Similarly, during frequency lock operation, the logic levels of the UPGATE and DOWNGATE commands are reversed. This results in the F_c pulses being applied to the count down input (pin 4) of A8A3A3IC1 for the duration of the DOWNGATE command. The remaining NAND gate of the count input logic provides F_c pulses to the clock input of the D-type flip-flop in A8A3A3IC19 (part of the zero count logic), when the output of 8-input NAND gate A8A3A3IC17 is a logical ONE level.

4-108. Up/Down Decade Counters A8A3A3IC1 through IC6. Each of these monolithic, TTL circuits is a synchronous reversible (up/down) BCD counter. The six counters are cascaded by feeding the carry and borrow outputs to the count up and count down inputs, respectively, of the suceeding counter. An active CLEAR command (logical ONE level) from the time base generator circuitry forces all the counter outputs (carry, borrow and Q_A through Q_D) to a logical ZERO level. The active LOAD input (logical ZERO level) from the zero count logic pre-sets all the counters (via the A through D inputs) to the number that is retained in the bistable storage latches.

4-109. Bistable Storage Latches A8A3A3IC7 through IC12. Each of these monolithic, TTL circuits is a 4-bit bistable latch consisting of four D-type edge-triggered flip-flops. The data inputs (Q_A through Q_D from the associated counter) are transferred to the Q outputs when an active STORE command (logical ONE level) from the time base generator circuitry is applied to the clock inputs. Each Q output follows the data input as long as the STORE command remains a logical ONE level. When this input goes to a logical ZERO level, the information (which was present at the data input at the time the transition occurred) is retained at the Q output until the STORE command returns to a logical ONE level.

TABLE 4-10. COUNT FREQUENCIES

RANGE MHz Switch Setting	fc
Internal Count Operation	
248-512	fo/8 (0.96875 - 2 MHz)
124-256	fo/16 (484.375 - 1000 kHz)
62-128	fo/32 (242.187 - 500 kHz)
31-64	fo/8 (0.96875 - 2 MHz)
15.5-32	fo/16 (484.375 - 1000 kHz)
7.75-16	fo/32 (242.187 - 500 kHz)
External Count Operation	
Any	10 Hz - 10 MHz

4-110. Zero Gates Logic. This logic consists of the six, quad-input negative NAND gates in A8A3A3IC14 through IC16. The 4-bit BCD outputs from the six counters (except the least significant bit of A8A3A3IC1) and the $\overline{\text{LOOP MODE}}$ input from the time base generator circuitry are applied to the zero gates logic. When all these inputs are a logical ZERO level, all six outputs of the ZERO gates logic are a logical ONE level. These six outputs are used by the zero count logic to generate the ZERO PULSE output.

4-111. Zero Count Logic. This logic consists of the following monolithic, TTL circuits: an 8-input positive NAND gate in A8A3A3IC17; a D-type edge-triggered flip-flop in A8A3A3IC19; and a monostable multivibrator (one-shot) in A8A3A3IC18. The six outputs of the zero gates logic are applied to the 8-input NAND gate, together with the least significant bit (Q_A) of the first decade counter (A8A3A3IC1) and the F_c pulses. When all these inputs to the 8-input NAND gate are a logical ONE level, its output switches to a logical ZERO level, thereby clearing the D-type flip-flop (see Figure 4-25). At the following cycle of the F_c, both the least significant bit and the clock input to the flip-flop go to a logical ZERO level. Since the flip-flop was previously cleared, it switches state when the clock pulse goes positive (which corresponds to zero count time). The resulting positive Q output of the flip-flop triggers the monostable multivibrator. When triggered, the one-shot produces a positive ZERO PULSE output of approximately 1.2 milliseconds. The R-C time constant of resistor A8A3A3R5 and capacitor A8A3A3C1 determine the pulse width. The negative $\overline{Q}$ output of the D-type flip-flop is the LOAD command which pre-sets the counters with the stored number.

4-112. FREQUENCY COUNTER DISPLAY CIRCUITRY. Figure 4-26.

4-113. Decoder/Drivers A8A3A2IC2, IC4, IC6, IC8, IC10 and IC12. These six monolithic, TTL circuits are BCD-to-seven segment decoder/drivers. Each circuit accepts a respective 4-bit BCD output from the counter/storage circuitry (paragraph 4-106) and, depending on the state of auxiliary inputs, decodes this data to drive the associated LED display. (Table 3-2 is a typical truth table for a seven-segment decoder/driver.) The circuits associated with the three most significant digits (A8A3A2IC8, IC10 and IC12) incorporate automatic leading and trailing-edge zero-suppression control (RBI and RBO), via the display logic in A8A3A2IC13 and IC14. Zero suppression of the three least significant digit circuits (A8A3A2IC2, IC4 and IC6) is inhibited by connecting their RBI terminals (pin 5) to the +5 volts DC supply.

4-114. LED Displays A8A3A2IC1, IC3, IC5, IC7, IC9 and IC11. Each of these solid-state circuits is a seven-segment numeric display with a decimal point (see Figure 4-27). A display rectangular segment is formed by reflection of the multidirectional red light from a light-emitting diode (LED). A logical ZERO level input causes current flow in an LED segment. The proper decimal point location is obtained either by applying a logical ZERO level $\overline{2DP}$, $\overline{3DP}$ or $\overline{4DP}$ signal from the control logic circuitry directly to the DP terminal (pin 6) of LED display IC3, IC5, or IC7, respectively; or by applying logical ONE level A + B and CS · $\overline{DS}$ signals from the control logic circuitry to a NAND gate in IC13, and coupling the resulting logical ZERO level output to the DP terminal of IC9.

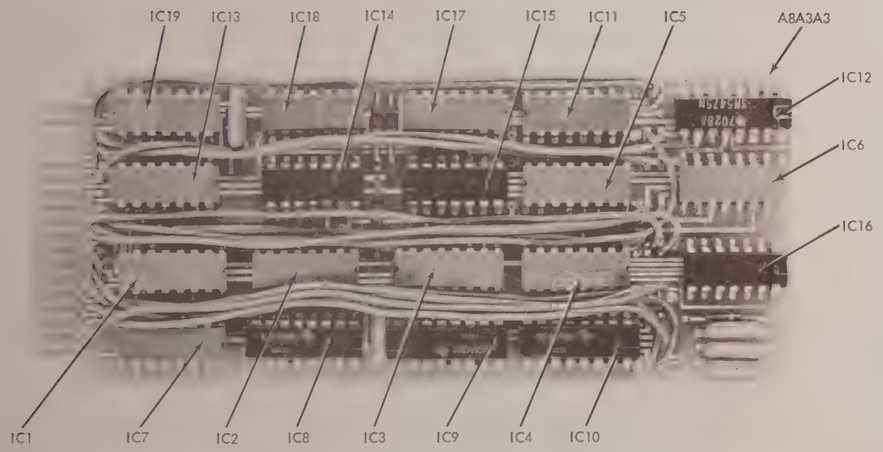
4-115. Display Logic. This logic consists of four, dual-input positive NAND gates and four inverters in A8A3A2IC13 and IC14. The display logic performs two major functions: it suppresses leading zeros, as necessary; and it controls the lighting of the proper range indicator (MHz or kHz). The zero suppression logic functions as follows. If the most significant digit is zero, the A + B and CS · $\overline{DS}$ inputs from the control logic circuitry (paragraph 4-125) are both a logical ZERO level, causing the output of a NAND gate in IC13 to be a logical ONE level. This, in turn, causes a logical ONE level to be applied to the DP terminal of IC9 and a logical ONE level level to be applied to the RBI terminal of IC12 (via an inverter in IC13). The result of this action is the holding off of a decimal point at the second most significant display (IC9); and the suppression of a zero indication at the most significant display (IC11). In a similar manner, a logical ZERO level output at the B 1/RBO terminal (pin 4) of IC10 or IC12 is gated with a logical ONE level $\overline{3DP}$ or $\overline{4DP}$ signal, respectively, from the control logic circuitry to suppress the zero indication at IC7 or IC9, when necessary. A logical ZERO level output is obtained at the BI/RBO terminal of IC10 or IC12 whenever a ZERO level is applied to its respective RBI terminal.

4-116. The lighting of the MHz and kHz indicators (DS2 and DS1, respectively) is controlled by a NAND gate in IC13. When the CS + DS and A + B logic signals are both a logical ONE level, a logical ZERO level is applied to the MHz indicator, causing it to light. At the same time, an inverter in IC13 causes a ONE level to be applied to the kHz indicator, keeping it turned off. When either of the inputs to the NAND gate is a logical ZERO level, the kHz indicator goes on and the MHz indicator goes off.

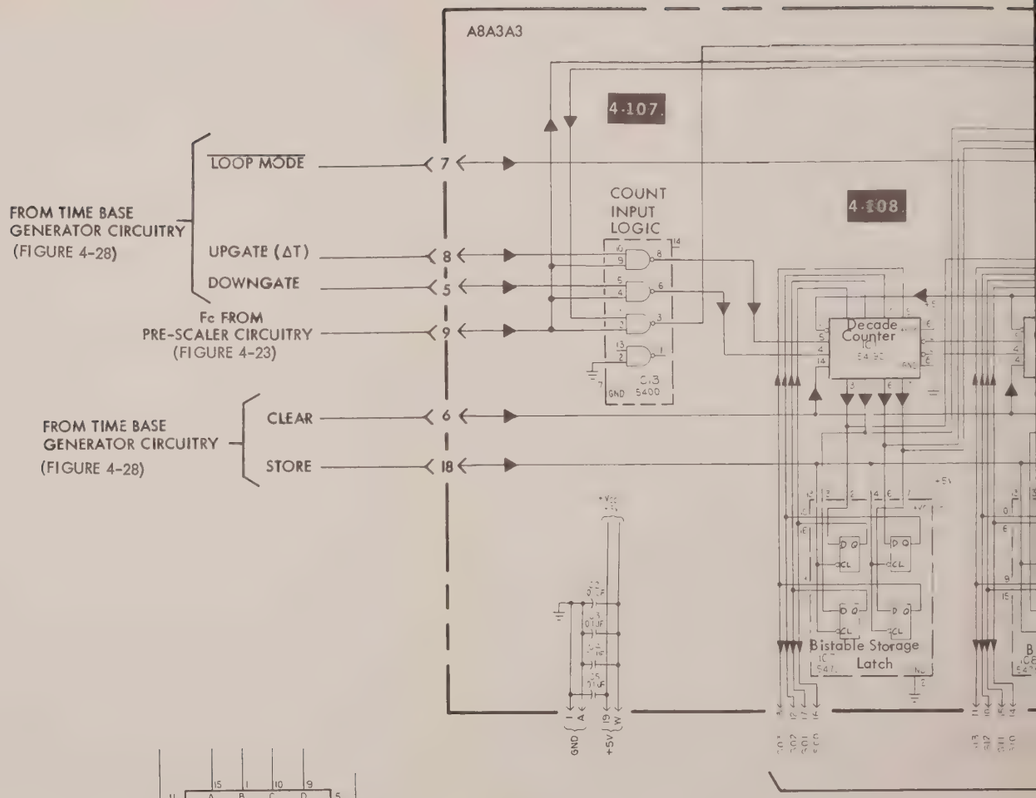
4-117. FREQUENCY COUNTER TIME BASE GENERATOR CIRCUITRY. Figure 4-28.

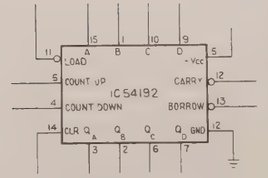
4-118. Internal 1 MHz Oscillator. This circuitry consists of 4 MHz crystal oscillator A8A3A6Q8, buffer amplifier A8A3A6Q7, and two monolithic, TTL, D-type edge-triggered flip-flops in A8A3A6IC4. The two D-type flip-flops are connected in cascade to divide the 4 MHz signal by four. Variable capacitor A8A3A6C8 provides fine frequency adjustment of the 4 MHz oscillator.

4-119. Frequency Divider. The divider consists of the following monolithic, TTL circuits: six J-K flip-flops in A8A3A5IC3, IC13 and IC14; six divide-by-two and six divide-by-five counters in A8A3A5IC6 through IC9, IC11, and IC12; two 4-line to 1-line data multiplexers (A and B) in A8A3A5IC10; and associated logic gates in A8A3A5IC2 and IC4. When rear-panel TIME BASE switch S2 is set to INT, the $\overline{\text{EXT STD}}$ signal is a logical ONE level. This allows the internal 1 MHz signal to be applied through a dual-input AND gate (which has the $\overline{\text{EXT STD}}$ signal as its other input) and an OR invert gate in A8A3A5IC2 to a dual-input positive NAND gate in IC4 and the clock input of a J-K flip-flop in IC3. Similarly, when the TIME BASE switch is set to EXT, the $\overline{\text{EXT STD}}$ signal is a logical ZERO level. This allows an external 1 MHz signal at rear-panel 1 MHz IN connector J8 to be applied through amplifier A8A3A5Q1, emitter follower A8A3A5Q2, a pulse shaper in A8A3A5IC1, and a dual-input AND gate and an OR gate in A8A3A5IC2 to the NAND gate in IC4 and the J-K flip-flop in IC3. The J-K flip-flop divides the selected 1 MHz signal by two, and the resulting



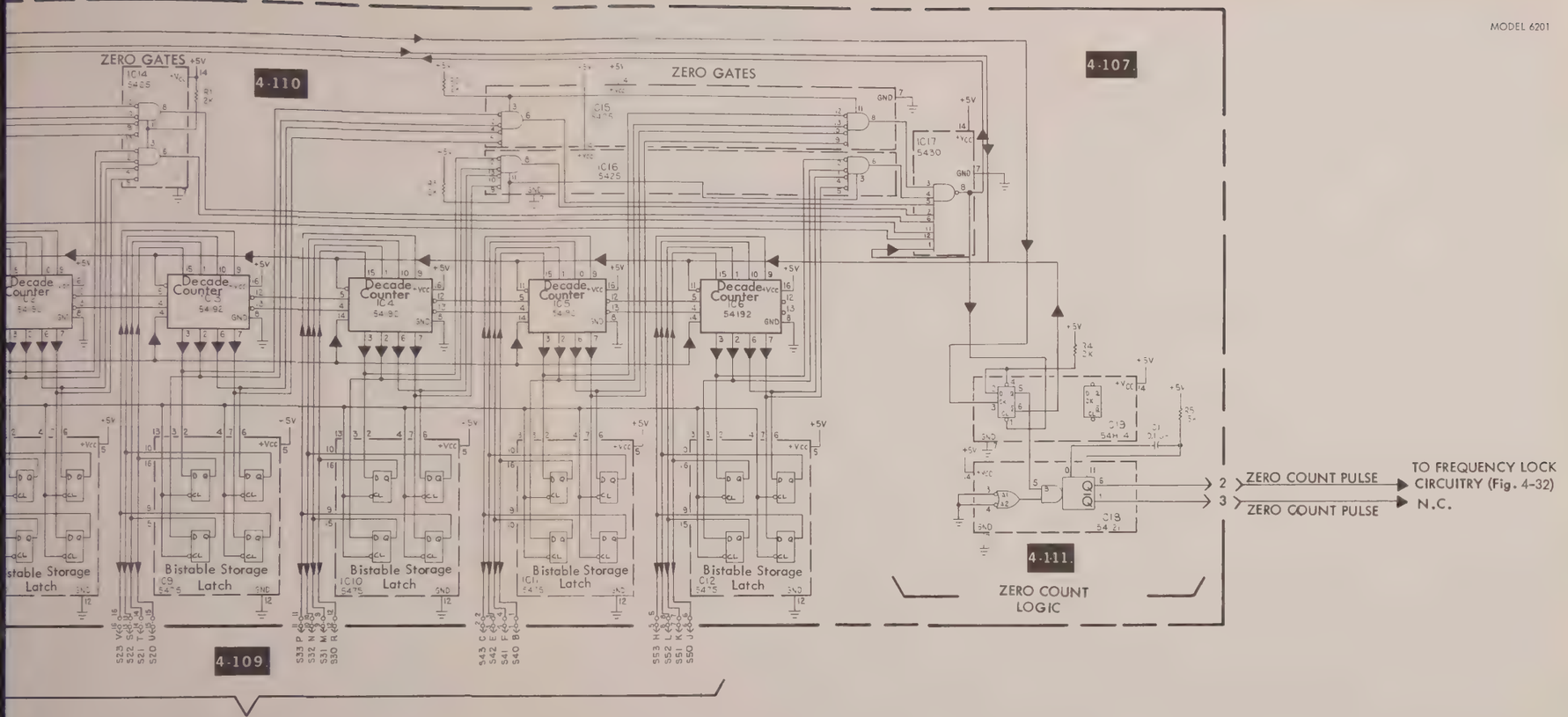
A8 A3 A3
Parts Locations





TYPICAL FOR DECADE COUNTERS IC1 THRU IC6

NOTES: UNLESS OTHERWISE NOTED
1. ALL RES ARE IN Ω, 1/4W, 5%
2. ALL CAPACITORS ARE 25V, ± 20%



24 LINE 4-BIT BDC OUTPUT TO DISPLAY CIRCUITRY (FIGURE 4-26)

Figure 4-24. Frequency Counter, Counter/Storage Circuitry, Functional Schematic Diagram

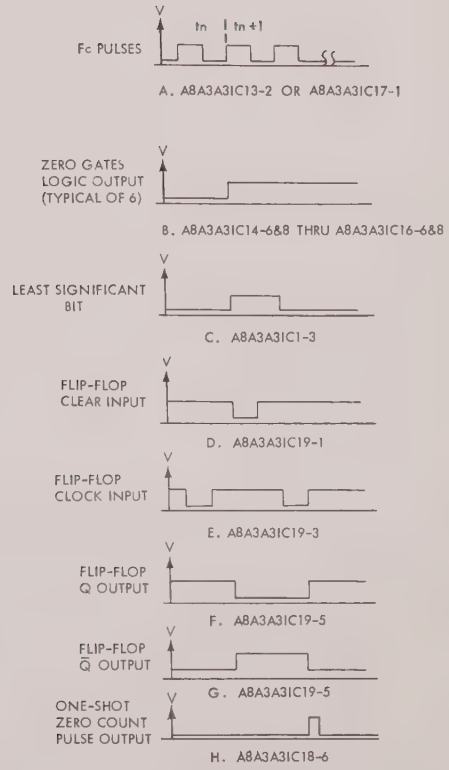
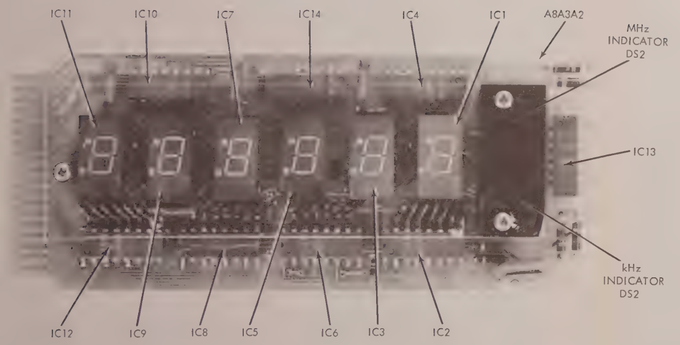
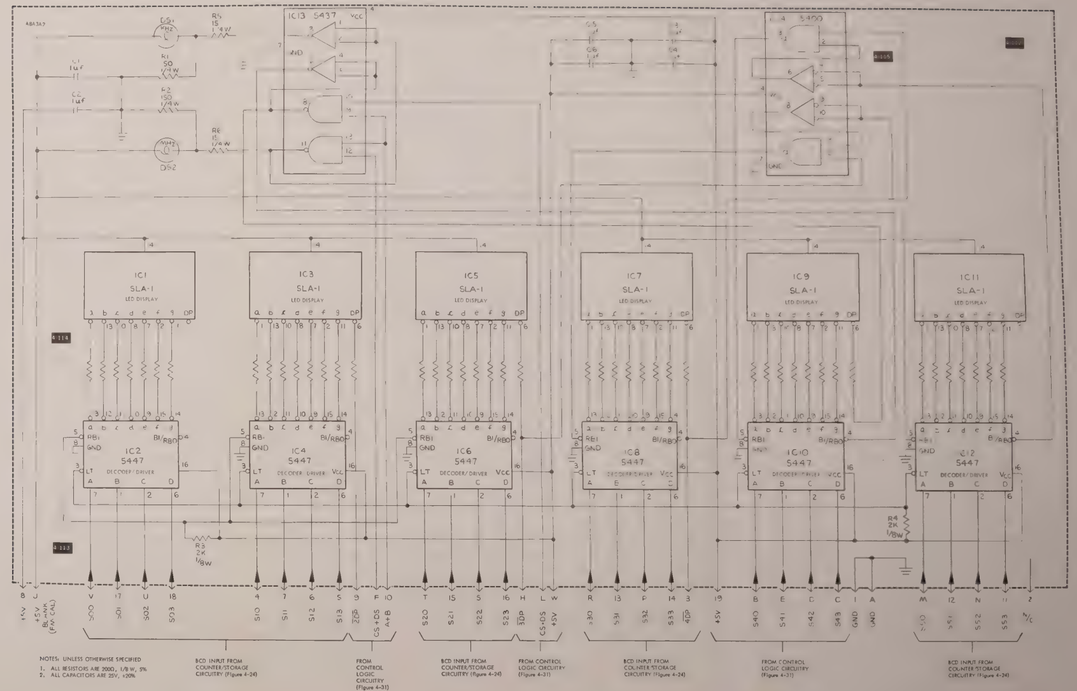


Figure 4-25. Zero Count Logic, Timing Diagram

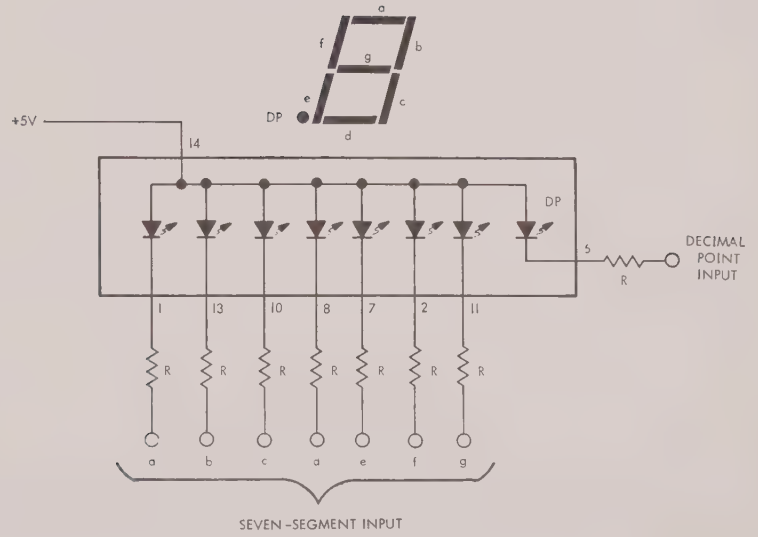


A8 A3 A2
Parts Locations



A8/A3/A2
4 -26.

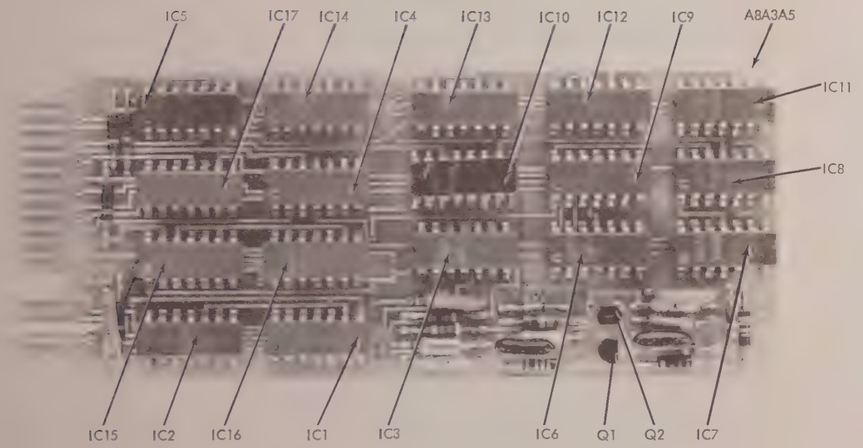
Figure 4-26. Frequency Counter Display Circuitry, Functional Schematic Diagram



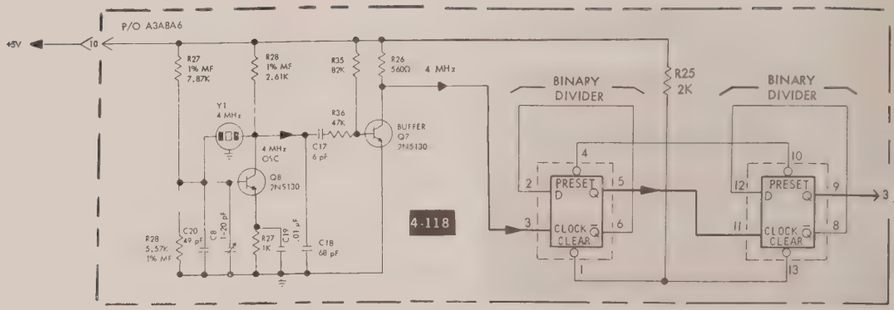
A8

4-27.

Figure 4-27. LED Display, Application Diagram



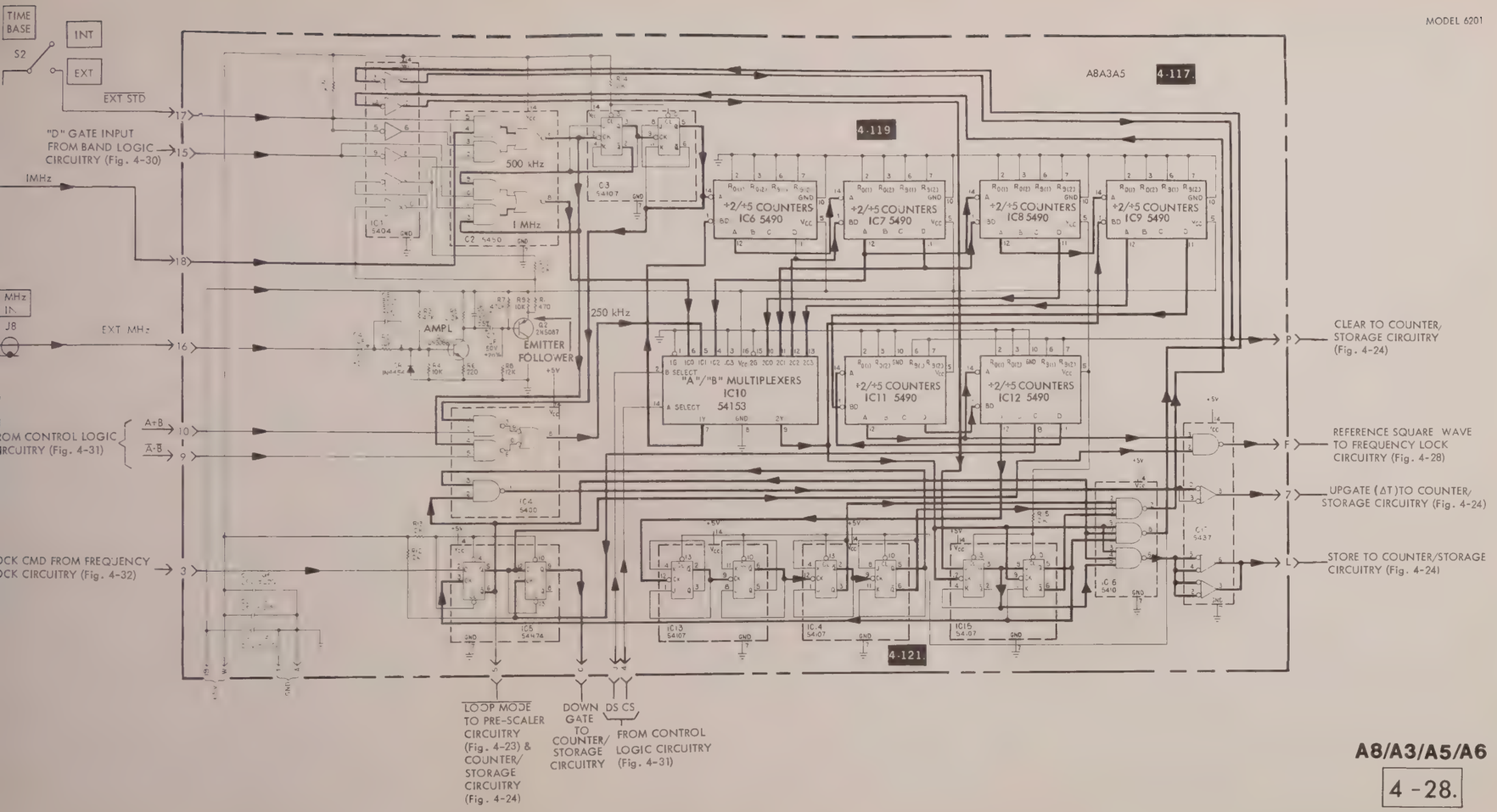
A8 A3 A5
Parts Locations



NOTES: UNLESS OTHERWISE NOTED
1. ALL RES. ARE IN Ω, 1/4W, 5%

TABLE 4-11. TIME BASE GENERATOR FREQUENCY DIVIDER DATA

RANGE MHz Switch Setting	A8A3A5IC2-8	A8A3A5IC4-8	A8A3A5IC10-7 (1 Y)	A8A3A5IC10-9 (2 Y)	A8A3A5IC17-8 (ΔT Gate)
248 - 512 MHz 124 - 256 MHz 62 - 128 MHz	500 kHz	250 kHz	0 VDC	15.625 kHz	256 msec
31 - 64 MHz 15.5 - 32 MHz 7.75 - 16 MHz	500 kHz	250 kHz	62.5 kHz	12.5 kHz	320 msec
31 - 64 MHz 15.5 - 32 MHz 7.75 - 16 MHz	500 kHz	250 kHz	0 VDC	15.625 kHz	256 msec
External Count					
0 - 9999.99 kHz (0.1 sec time base)	1 MHz	1 MHz	1 MHz	40 kHz	100 msec
0 - 9999.99 kHz (1 sec time base)	500 kHz	1 MHz	500 kHz	4 kHz	1000 msec



A8/A3/A5/A6

4 - 28.

Figure 4-28. Frequency Counter Time Base Generator Circuitry, Functional Schematic Diagram

500 kHz output is simultaneously applied to another divide-by-two, J-K flip-flop in IC3 and a second dual-input AND gate in IC2. The 250 kHz output of the second J-K flip-flop is, in turn, simultaneously applied to a second dual-input NAND gate in IC4 and the first stage of four divide-by-two counters in IC6 through IC9 (via input and output pins 14 and 10, respectively, of each IC). The resulting 62.5 kHz output of IC7 is then applied to the A multiplexer in IC10, together with the selected outputs of gate logic in IC2 and IC4 and a ZERO level input (via pins 3 through 6 of IC10). The outputs selected by the gate logic in IC4 and IC5 (and the A and B multiplexers) dpends on the setting of the RANGE MHz selector switch and FM CAL pushbutton S3 in the internal count mode; and the setting of the INT TIME BASE switch in the external count mode (refer to Table 4-11).

4-120. The 1Y signal output of the A multiplexer (which is present at pin 7 of IC10) is applied to the first stage of three divide-by-five counters in IC6 through IC8 (via input and output pins 1 and 11, respectively, of each IC). The resulting outputs of these counters are, in turn, applied to the B multiplexer in IC10, together with the 15.625 kHz output of the divide-by-two counter in IC9 (via pins 10 through 13 of IC10). The 2Y signal output of the B multiplexer (which is present at pin 9 of IC10) is then applied to the input of a divide-by-8000 chain consisting of the following: three divide-by-five counters in IC9, IC11 and IC12; two divide-by-two counters in IC11 and IC12; and four divide-by-two, J-K flip-flops in IC13 and IC14. The resulting output of IC14 is applied to a two-input positive NAND gate in IC4. When in the normal (unlocked) count mode, the other input to this NAND gate ($\overline{\text{LOOP MODE}}$) is at an enabling logical ONE level. The gated output of IC4 is applied to an inverter in IC17 and the resulting UPGATE (ΔT) output is applied to the counter/storage circuitry (paragraph 4-106).

4-121. Time Base Logic. This logic consists of the following monolithic, TTL, circuits: two divide-by-two J-K flip-flops in IC15; two D-type edge-triggered flip-flops in IC5; three 3-input positive NAND gates in IC16; one dual-input positive NAND gate in IC17; and four inverters in IC17. When in the normal (unlocked) count mode, the Q ($\overline{\text{LOOP MODE}}$) output of a D-type flip-flop in IC5 is a logical ONE level. This output enables a NAND gate in IC4 and two NAND gates in IC16, thereby obtaining the UPGATE (ΔT) output, and allowing the generation of the STORE and CLEAR commands (as described below). At this time, the ZERO level $\overline{Q}$ output of the D-type flip-flop is simultaneously applied to a NAND gate in IC17 and the second D-type flip-flop in IC5, thereby disabling the generation of the reference square wave signal and the DOWNGATE command. Similarly, when in the frequency lock mode, the ONE level LOCK command from the frequency lock circuitry (paragraph 4-127) causes the Q and $\overline{Q}$ outputs from the first D-type flip-flop in IC5 to be reversed. This results in the generation of the reference square wave signal and DOWNGATE command (as described below), and the disabling of the UPGATE, STORE and CLEAR commands.

4-122. The STORE and CLEAR commands are generated by a feedback loop consisting of the three NAND gates in IC16 and the two divide-by-two J-K flip-flops in IC15 as follows (see Figure 4-29). The 2Y/4000 output and 2Y/8000 output (complement of the ΔT gate) from the J-K flip-flops in IC14 are applied to a NAND gate in IC16. Also applied to this NAND gate is the $\overline{Q}$ output of the second J-K flip-flop in IC15. When all three inputs to the NAND gate in IC16 are a logical ONE level, a logical ONE level is applied to the J input of the first J-K flip-flop in IC15 via an inverter in IC1. (As shown in the timing diagram of Figure 4-24, this condition occurs coincident with the trailing edge of the ΔT gate.) The resulting output of the first J-K flip-flop is, in turn, simultaneously applied to the J input of the second J-K flip-flop in IC15 and a NAND gate in IC16 (together with the $\overline{\text{LOOP MODE}}$ and 2Y signals). The resulting Q output of the second J-K flip-flop is simultaneously applied to a NAND gate in IC17 (together with the $\overline{\text{LOOP MODE}}$ and 2Y signals) and the clock input of a D-type flip-flop in IC5. When in the normal (unlocked) count mode, the subsequent gating action of the two NAND gates in IC16 produces a STORE command output from an inverter in IC1 which immediately follows the ΔT gate; and a CLEAR command from an inverter in IC17 which immediately follows the STORE command. The duration of these commands is equal to the 2Y signal divided-by-2. Similarly, the reference square wave is generated at a NAND gate in IC17 during the frequency locked mode, using the 2Y divided-by-250 output of a divide-by-two counter in IC11. The DOWNGATE command (logical ONE level) is generated at the Q output of a D-type flip-flop in IC5 whenever a ONE level LOCK command is applied to its D input (via the other D-type flip-flop in IC5).

4-123. FREQUENCY COUNTER BAND LOGIC CIRCUITRY. Figure 4-30.

4-124. This circuitry consists of the following monolithic, TTL, circuits: four, dual-input NOR gates in A5A3IC1; and four inverters in A5A3IC2. In the normal internal count mode, the band logic circuitry converts the RANGE MHz selector switch position to a 4-bit binary code output (refer to Table 3-4) as described in paragraph 3-77. Similarly, in the external count mode, the circuitry converts the positions of the rear-panel INT TIME BASE switch and the front-panel EXT COUNT pushbutton to a 4-bit binary code output. Isolation diodes A5A3CR1, A5A3CR5 and A5A3CR9 prevent damage to the inverters in A5A3IC1.

4-125. FREQUENCY COUNTER CONTROL LOGIC CIRCUITRY. Figure 4-31.

4-126. This circuitry consists of the following monolithic, TTL circuits: three inverters in A8A3A4IC5; four dual-input negative NAND gates in A8A3A4IC6; two dual-input positive NAND gates in A8A3A4IC8; three dual-input NOR gates in A8A3A4IC9; and two dual-input positive NAND gates, a dual-input NOR gate, and an inverter in A8A3A4IC10. The circuitry provides the necessary logical gating to convert the 4-bit binary code signal from the band logic circuitry (paragraph 4-123) into logic outputs which control the following functions:

Logic Output	Function
A + B	Display Range Lights
$\overline{A}$ + B	Time Base Gate Period
$\overline{A}$ · $\overline{B}$	Time Base Gate Period
DS	Time Base Gate Period
CS	Time Base Gate Period
CS · $\overline{DS}$	Display Range Lights
$\overline{4DP}$	Display, Decimal Point
$\overline{3DP}$	Display, Decimal Point
$\overline{2DP}$	Display, Decimal Point
CS + DS	Display Range Lights

Table 3-5 lists the gate logic outputs from the control logic circuitry for the normal internal count mode and the external count mode.

4-127. FREQUENCY LOCK CIRCUITRY. Figure 4-32.

4-128. Frequency Lock Flip-Flop. This flip-flop circuit consists of two monolithic, TTL, inverters in A5A3IC2 and associated components. The two inverters are connected in a bistable latch configuration by feeding back the output from one inverter to the input of the other, via diodes A5A3CR7 and A5A3CR10. The set input (pin 9) of the flip-flop is connected to isolation diode A5A3CR6; the reset input (pin 11) is connected to isolation diodes A5A3CR3, A5A3CR4, A5A3CR8 and A5A3CR15 (which comprise an OR gate). Applying a ground (logical ZERO level) to the cathode of any of the isolation diodes places the flip-flop in the respective state. When the flip-flop is placed in the set (locked) state, a logical ONE and logical ZERO are obtained at pins 8 and 10, respectively, of IC2. This results in current flow through the LOCK indicator (LED DS1), causing it to light.

4-129. Transistor Switch A5A5Q1. This stage is normally held at cutoff by the application of a logical ZERO level (ground) from the wiper arm of A5A5S1-B (part of RANGE MHz switch) to its base. However, when the RANGE MHz switch position is changed, this ground input is momentarily replaced by +5 volts DC through A5A5R13. This causes Q1 to saturate, momentarily applying a ZERO level to the reset input (via CR4) of the flip-flop. Thus, the frequency lock flip-flop is placed in the reset state whenever the RANGE MHz switch position is changed.

4-130. Automatic Frequency Lock Circuit. The following subparagraphs describe the stages of the automatic frequency lock circuit.

4-131. Lock Control Logic. This logic consists of a monolithic, TTL, D-type edge-triggered flip-flop in A8A3A7U1. The ZERO count pulse from the counter/storage circuitry (paragraph 4-100) is applied to its clock input. In the frequency lock mode, flip-flop A5A3IC2 is in the set (locked) state, causing a logical ONE level to be simultaneously applied to the D and clear inputs (pins 1 and 2) of the lock control flip-flop. This results in a logical ZERO level output at its $\overline{Q}$ terminal (pin 6). Similarly, in the normal count (unlocked) mode, the frequency lock flip-flop is in the reset (unlocked) state, causing a logical ZERO level to be simultaneously applied to the D and clear inputs of the lock control flip-flop. This results in a logical ONE level output at its $\overline{Q}$ terminal.

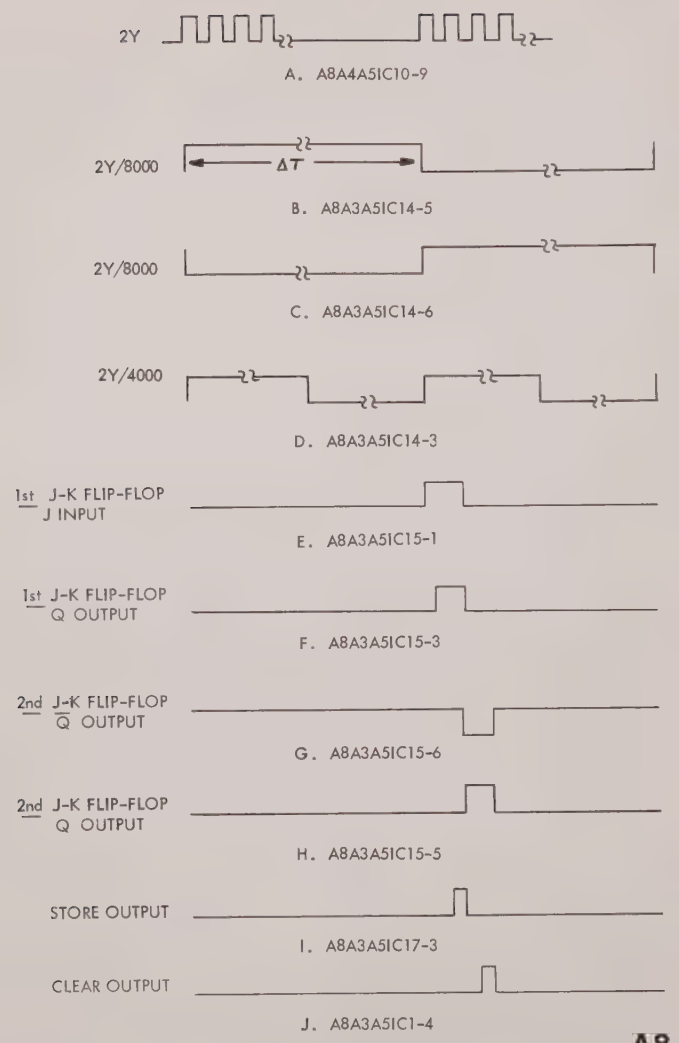
4-132. Lock/Unlock Driver A8A3A7Q1 and Switch A8A3A7Q2. Stage Q1 is a switching transistor and stage Q2 is an FET switch. In the normal (unlocked) count mode, the logical ONE level output of the lock control logic flip-flop turns Q1 off and Q2 on. Under this condition, the front-panel VERNIER frequency control (which is connected to the -26 volts DC supply through A8A3A7R6 and R7) controls the drain voltage of Q2, and ultimately the gate voltage of FET A8A3A7Q6. Similarly, when in the frequency lock mode, the ZERO level output of the lock control logic flip-flop turns Q1 on and Q2 off, thereby disconnecting the VERNIER frequency control from the gate circuit of Q6.

4-133. Buffer Amplifier A8A3A7Q7. This stage is a switching transistor which is turned on in the normal count mode. This produces an output which turns off the succeeding zero pulse sample switch stage (A8A3A7Q4). In the frequency lock mode, the positive ZERO count pulse from the counter/storage circuitry turns Q7 off, thereby turning on Q4 for the duration of the ZERO count pulse.

4-134. Lock Ramp Generator. This stage is composed of switching transistor A8A3A7Q3 and FET A8A3A7Q5. In the normal count mode, transistor Q3 is turned off and capacitor A8A3A7C3 is charged to -26 volts DC through resistors A8A3A7R10 and A8A3A7R11. This results in a Q5 output of approximately -5 volts DC across A8A3A7R13. In the frequency lock mode, the +5 to 0 volts DC reference square wave from the time base generator circuitry alternately turns Q3 on and off, thereby producing a -5V to -15V triangular wave output from Q5.

4-135. Zero Pulse Sample Switch A8A3A7Q4. This stage is an FET switch which is held at cutoff during the normal count mode by the output of Q7. In the frequency lock mode, the -5V to -15V triangular wave output of Q5 is applied to the zero pulse sample switch, together with the negative ZERO count pulse output from Q7. Each ZERO count pulse turns on Q4, allowing the timing of the ZERO pulse to be compared with the instantaneous voltage of the triangular wave. The ZERO count pulse samples the triangular wave on the negative-going slope. When the master oscillator frequency is constant, the ZERO count pulse will always sample the triangular wave at the same point. However, if the oscillator frequency increases or decreases, the ZERO count pulse occurs sooner or later, respectively, and the voltage sampled on the triangular wave is more positive or negative, respectively. The resulting Q4 output (which is equal to the triangular voltage at the ZERO count pulse) is stored by capacitor A8A3A7C5 of the succeeding sample and hold circuit.

4-136. Sample and Hold Circuit A8A3A7Q6. This stage is an FET source follower which provides an AFC/vernier output of approximately -9 to -11 volts DC to tune the master oscillator over a range of approximately 250 kHz. The actual control range is about 0.1% of any particular frequency range. In the normal count mode, the Q6 output is determined by the setting of the front-panel VERNIER frequency control. In the frequency lock mode, the Q6 output is determined by the output from the zero pulse sample switch.



A8

4 - 29.

Figure 4-29. STORE and CLEAR Commands Generation, Timing Diagram

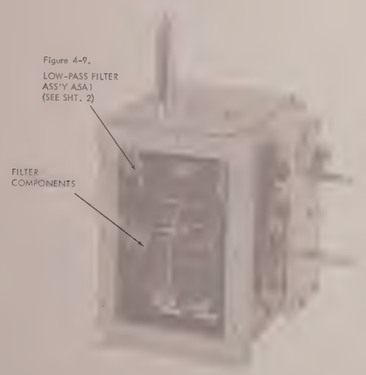
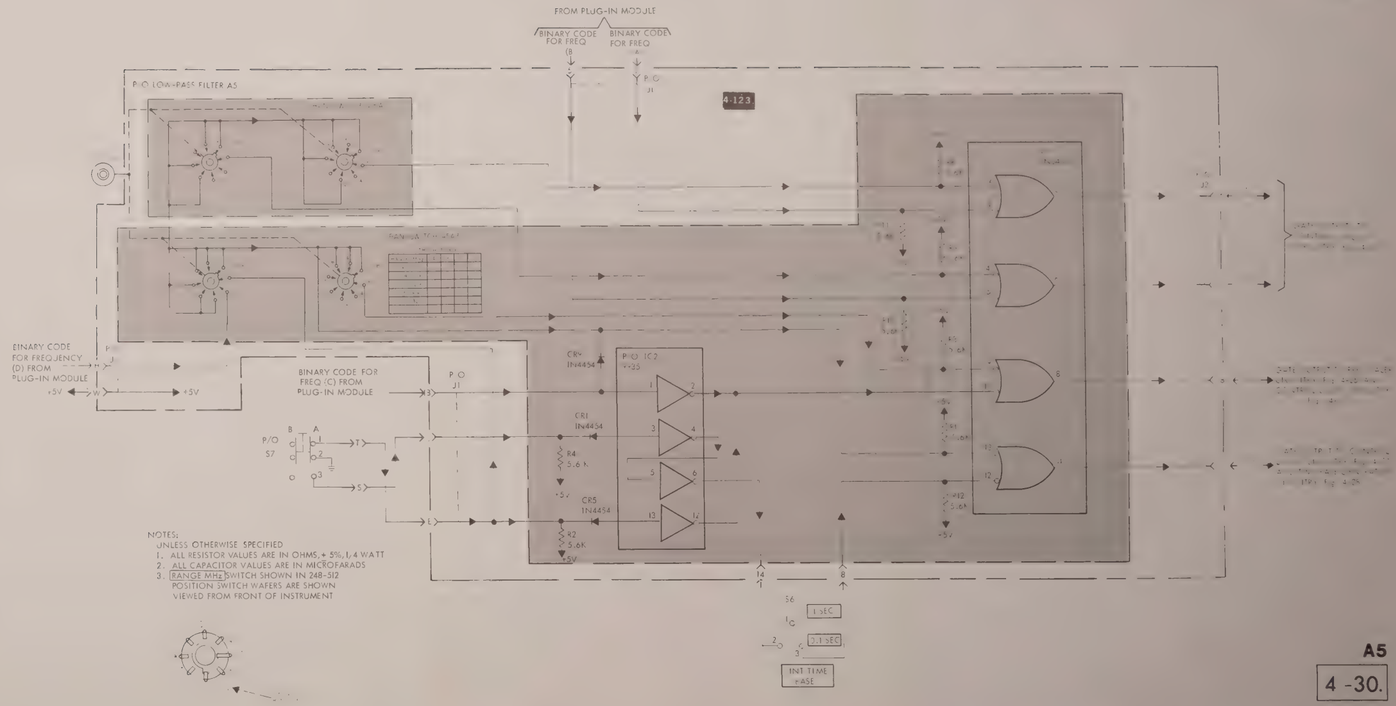


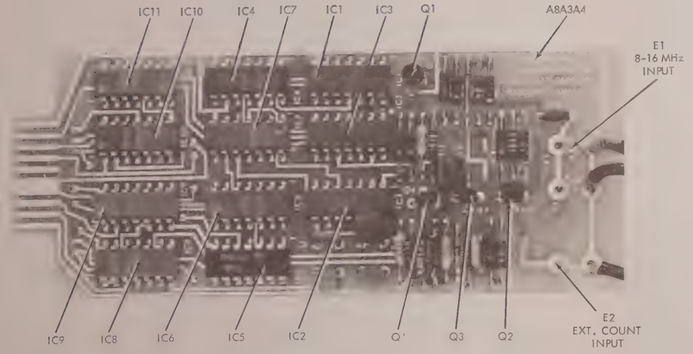
Figure 4-9.
LOW-PASS FILTER ASS'Y A5A1 (SEE SHT. 2)

A5
Parts Locations

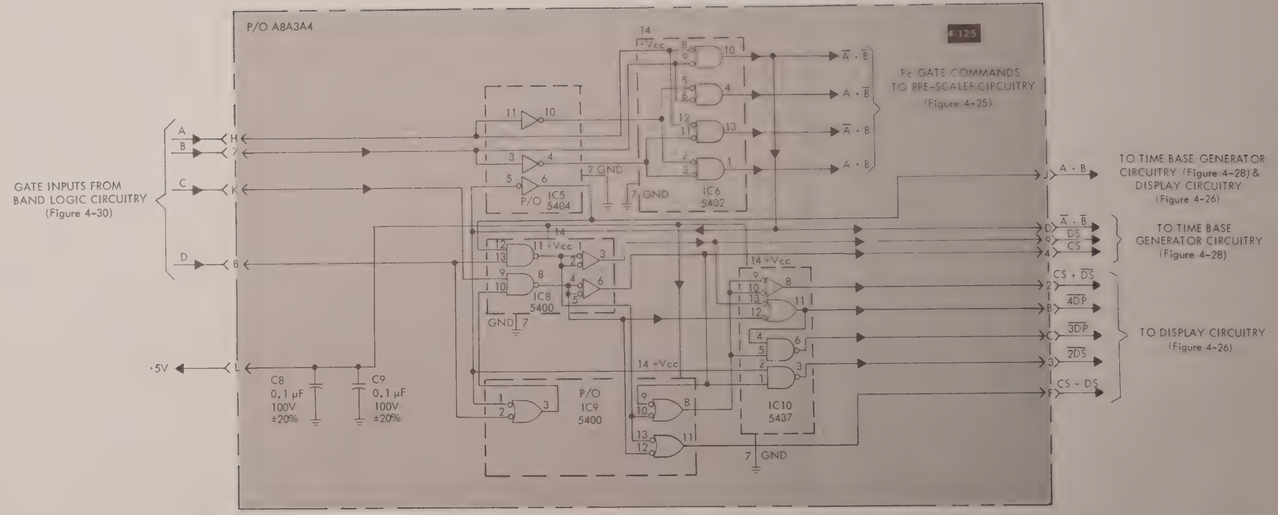


A5
4 -30.

Figure 4-30. Frequency Counter Band Logic Circuitry, Functional Schematic Diagram

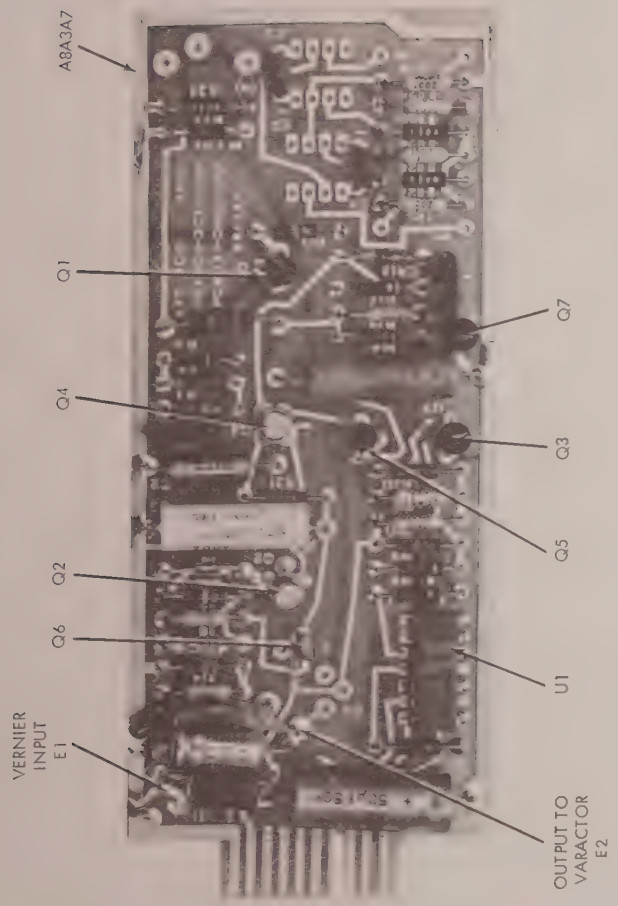


A8 A3 A4
Parts Locations



A8 A3 A4
4 - 31.

Figure 4-31. Frequency Counter Control Logic Circuitry, Functional Schematic Diagram



A8 A3 A7
Parts Locations

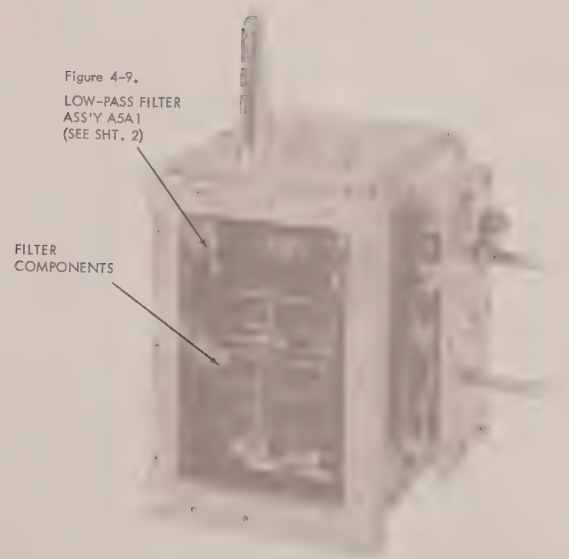
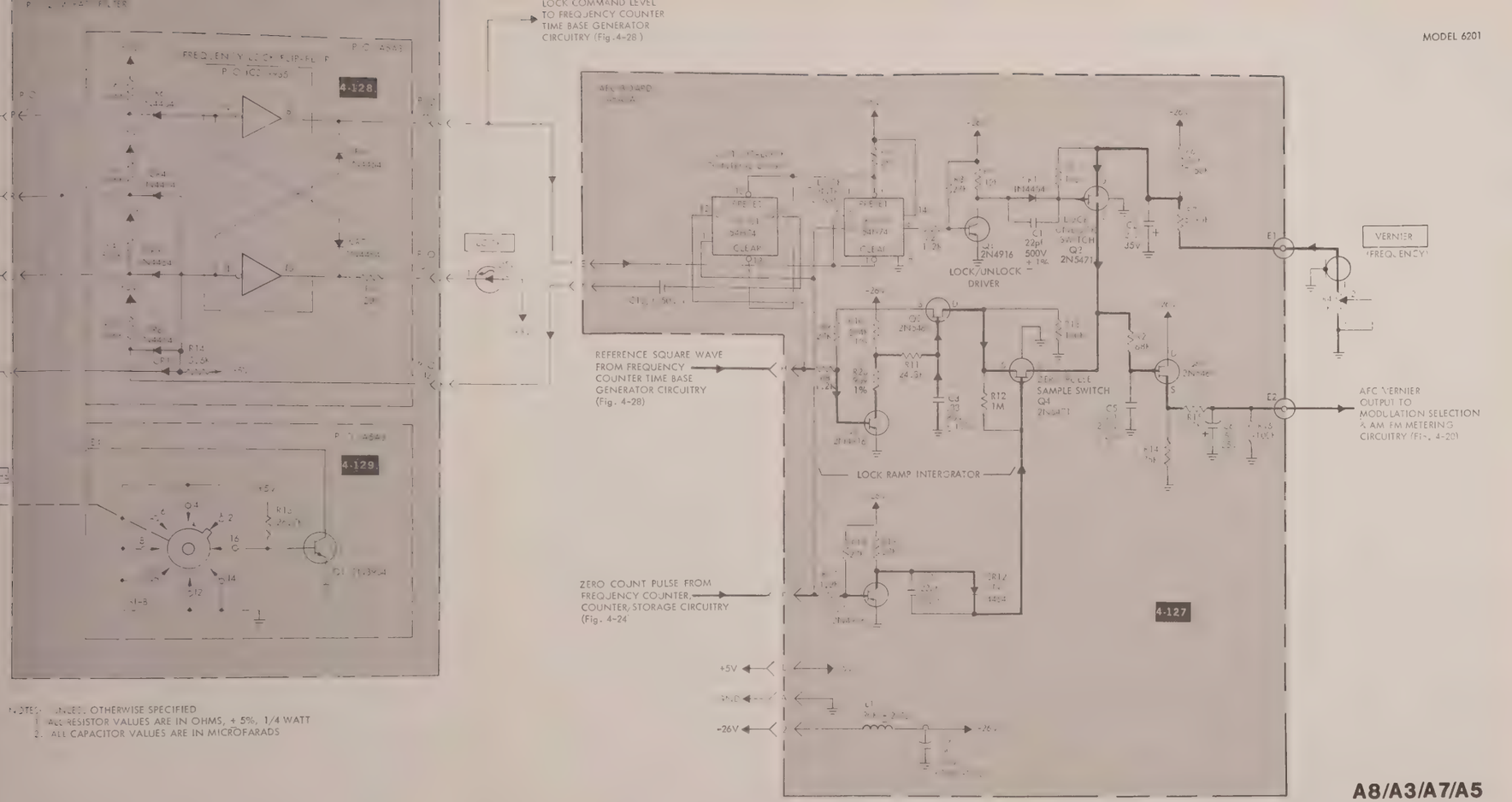


Figure 4-9.
LOW-PASS FILTER ASS'Y A5A1 (SEE SHT. 2)



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS, ± 5%, 1/4 WATT
2. ALL CAPACITOR VALUES ARE IN MICROFARADS

A8/A3/A7/A5

4-32.

Figure 4-32. Frequency Lock Circuitry, Functional Schematic Diagram

4-137. Out-of-Lock Control Logic. This logic consists of a monolithic, TTL, D-type edge-triggered flip-flop in A8A3A7U1. The out-of-lock control logic functions as follows. The stable reference square wave is applied to the D input of the flip-flop and the ZERO count pulse is applied to its clock input. When the master oscillator frequency is in the lock capture range, the ZERO count pulse always occurs while the reference square wave is a logical ONE level. However, when the master oscillator frequency drifts out of the capture range, the ZERO count pulse occurs while the reference square wave is a logical ZERO level. This results in a negative pulse output from the out-of-lock logic which places frequency lock flip-flop A5A3IC2 in the unlocked state. Whenever this flip-flop is in the unlocked state, a logical ZERO level is applied to the lock control logic in A8A3A7U1, turning on lock/unlock switch A8A3A7Q2. This, in turn, connects the VERNIER frequency control to the input of the sample and hold stage, thereby allowing vernier control of the master oscillator frequency.

4-138. REGULATED POWER SUPPLIES. Figure 4-33.

4-139. -26 Volt Regulated Supply. This supply consists of full-wave bridge rectifier A9A1CR5, filter capacitor A9A1C1, and a current-limiting voltage regulator consisting of difference amplifier A9A2Q3, driver A9A2Q5, series regulator A9Q1, current limiter A9A2Q2 and associated circuitry. The full-wave rectifier and filter provide the unregulated power to drive the regulator. The output level of the regulator is set at -26 volts DC by screwdriver control A9A2R7. The reference voltage for the difference amplifier is obtained from zener diode A9A2CR4. A pre-regulated $-V_{CC}$ supply for section A of the dual-transistor difference amplifier is provided by zener diode A9A2CR1. Any variation in the output voltage due to changes in current drawn from the supply and/or fluctuations in available line voltage are sensed and amplified by the difference amplifier. An error voltage is coupled through the driver (an emitter follower) to the series regulator, the latter changing it dynamic resistance in the direction which returns the output voltage to its preset level of -26 volts. Current limiting is achieved by A9A2Q2 in conjunction with resistor A9A2R9. Should more than the nominally 0.25 ampere be drawn from the supply, the voltage across A9A2R9 will drive A9A2Q2 into its linear region of operation, effectively reducing the gain of the difference amplifier. This, in turn, limits the current passed by the series regulator, even during short circuit conditions. Zener diode A9A2CR2 provides a regulated -12 volt output which is used as the -V supply by the IC difference amplifiers in the remaining supplies.

4-140. +12 Volt Regulated Supply. This supply consists of full-wave bridge rectifier A9A1CR6, filter capacitor A9A1C2, difference feedback amplifier A9A2IC1, driver A9A2Q1, series regulator A9Q4, and current limiter A9A2Q8. The output level of the supply is set at +12 volts by screwdriver control A9A2R17 and the reference voltage for the IC difference amplifier is obtained from the -26 volt supply via the voltage divider consisting of A9A2R18, A9A2R17 and A9A2R37. The +V supply for the IC difference amplifier is provided by zener diode A9A2CR5 and the -V supply for this amplifier is provided by the -26 volt power supply. Operation of this supply is similar to the -26 volt supply, except that current limiting occurs at nominally 1.5 amperes.

4-141. +6 Volt Regulated Supply. This supply consists of full-wave bridge rectifier A9A1CR1 through CR4, filter capacitor A9C1, difference feedback amplifier A9A2IC4, series regulator A9Q3, and current limiter A9A2Q17. The output level of the supply is set at +6 volts by screwdriver control A9A2R35 and the reference voltage for the IC difference amplifier is obtained from the +12 volt supply via the voltage divider consisting of A9A2R34 through R36. The +V and -V supplies for the IC difference amplifier are provided by the +12 volt supply and -26 volt supply, respectively. Operation of this supply is similar to the -26 volt supply, except that current limiting occurs at nominally 0.35 ampere.

4-142. +5 Volt Regulated Supply. This supply contains the same full-wave bridge rectifier and filter capacitor as the +6 volt supply, difference feedback amplifier A9A2IC3, driver A9Q2, parallel series regulators Q1 and Q2 (rear-panel mounted), and current limiter A9A2Q15. The output level of the supply is set at +5 volts by screwdriver control A9A2R29 and the reference voltage for the IC difference amplifier is obtained from the -26 volt supply via the voltage divider consisting of A9A2R31, A9A2R29 and A9A2R38. The +V and -V supplies for the IC difference amplifier and provided by the +12 volt supply and -26 volt supply, respectively. Operation of this supply is similar to the -26 volt supply, except that current limiting occurs at nominally 4 amperes.

4-143. -5.2 Volt Regulated Supply. This supply contains the same full-wave bridge rectifier as the +5 and +6 volt supplies, filter capacitor A9A1C3, difference feedback amplifier A9A2IC2, driver A9A2Q10, series regulator A9Q5, and current limiter A9A2Q11. The output level of the supply is set at -5.2 volts by screwdriver control A9A2R23 and the reference voltage for the IC difference amplifier is obtained from the -26 volt supply via the voltage divider consisting of A9A2R23 through R25. The +V and -V supplies for the IC difference amplifier are provided by the +12 volt supply and -26 volt supply, respectively. Operation of this supply is similar to the -26 volt supply, except the current limiting occurs at nominally 1.2 amperes.

4–144. REMOVAL PROCEDURES.

4-145. Paragraphs 4-146 through 4-156 detail the procedures for removing the major assemblies from the main chassis. Replacement is accomplished by following the reverse of the procedure.

4-146. MASTER OSCILLATOR A1.

a. Remove frequency counter A8 as directed in paragraph 4-155.

b. Loosen and remove the seven screws that secure the brace, to the low-pass filter assembly, main chassis mounting block and side of plug-in housing. Withdraw brace from main chassis.

c. Disconnect A2A1 from A1J1 and disconnect P4 from A1J2.

d. Unsolder the orange and black leads of the twisted pair from feedthrough capacitor A1C1 and the ground lug at the base of the feedthrough, respectively (see Figure 4-1).

e. Loosen the two setscrews that secure the FREQUENCY control knob to the master oscillator tuning shaft; remove the knob.

f. Stand the Signal Generator on its left side and loosen (but do not remove) the four screws that secure A1 to the main chassis bottom plate. Place the Signal Generator rightside-up and then lift the right side of the instrument and remove the four screws loosened earlier. Lower the Signal Generator and carefully withdraw the master oscillator assembly.

4-147. FREQUENCY DIVIDER A2.

a. Disconnect A2P1 and A4P1 from A1J1 and A5A1J1, respectively. Set the RANGE MHz switch to 62-128.

b. Place the Signal Generator upside-down and loosen (but do not remove) the four screws that secure A2, A3 and A4 (mechanically joined by 12 screws) to the main chassis bottom plate. Place the Signal Generator rightside-up and then lift the rear of the instrument and remove the four screws loosened earlier. Lower the Signal Generator.

c. Place a sheet of cardboard (approximately 1 foot square) on the left-rear corner of the Signal Generator frame. Carefully lift A2, A3 and A4 from the main chassis bottom plate and place the joined assemblies atop the cardboard.

d. Loosen and remove the six screws that secure A2 to A3; the frequency divider assembly can now be separated from A3. Disconnect A3A2P1 from A2J1.

e. Loosen and remove the three screws that secure the shield plate to A2. Carefully separate the shield plate from A2, taking care not to unseat the RF gasketing. The components and subassemblies within A2 will be visible and accessible (see Figure 4-4).

f. To remove A2 completely, disconnect W2P1 and !6 from A2J2 and A2J3, respectively. Unsolder the red +12 volt lead (from A3C1) of the red/green twisted pair at A2A5C2. Unsolder the green -5.2 volt lead (from A3C2) of the red/green twisted pair at A2A5C1.

4-148. MODULATOR A3.

a. Perform steps a through d of paragraph 4-147.

b. Perform steps b and c of paragraph 4-149.

c. Separate both A2 and A4 from A3. The components and subassemblies within the modulator will be visible and accessible (see Figure 4-5).

d. For complete removal of A3, perform step f of paragraph 4-149 and then disconnect W1P1, and A6P1 from A3J3, and A3J2, respectively. Unsolder the red +12 volt lead and the green -5.2 volt lead from their terminations within A3.

4-149. WIDEBAND POWER AMPLIFIER A4.

a. Perform steps a through d of paragraph 4-147.

CAUTION

Do not attempt to separate A4 from A3 before first disconnecting A3A2P2 from A4A1J1.

b. Loosen and remove the six screws that secure A4 to A3 and carefully separate A4 from A3 by approximately one inch. Using a pair of long nose pliers, carefully disconnect A3A2P2 from A4A1J1.

c. Separate A4 from A3, taking care not to unseat the RF gasketing. The components within A4 will be visible and accessible (see Figure 4-7).

d. To remove A4 completely, unsolder the red +12 volt lead at A3A5C1. Unsolder the green -5.2 volt lead at A3A5C2.

4-150. LOW-PASS FILTER A5.

a. Loosen (but do not remove) the four screws that secure the low-pass filter to the main chassis bottom plate.

b. Set the RANGE MHz switch fully clockwise to 248 - 512 and loosen the setscrews on the coupling which joins the RANGE MHz shaft of the low-pass filter rotor. Slide the coupling onto the rotor shaft.

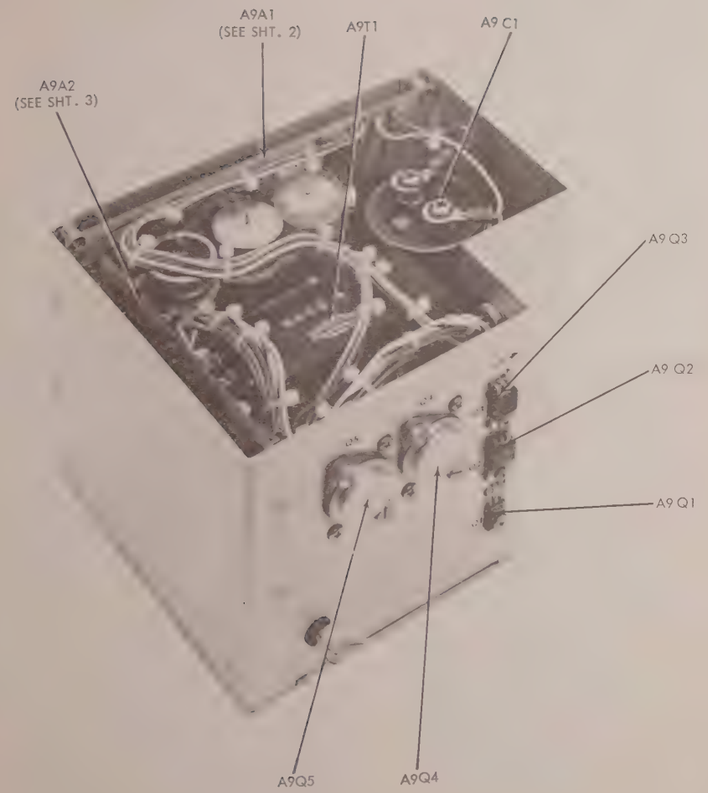
c. Unsolder the single blue lead from A5A1A5C1.

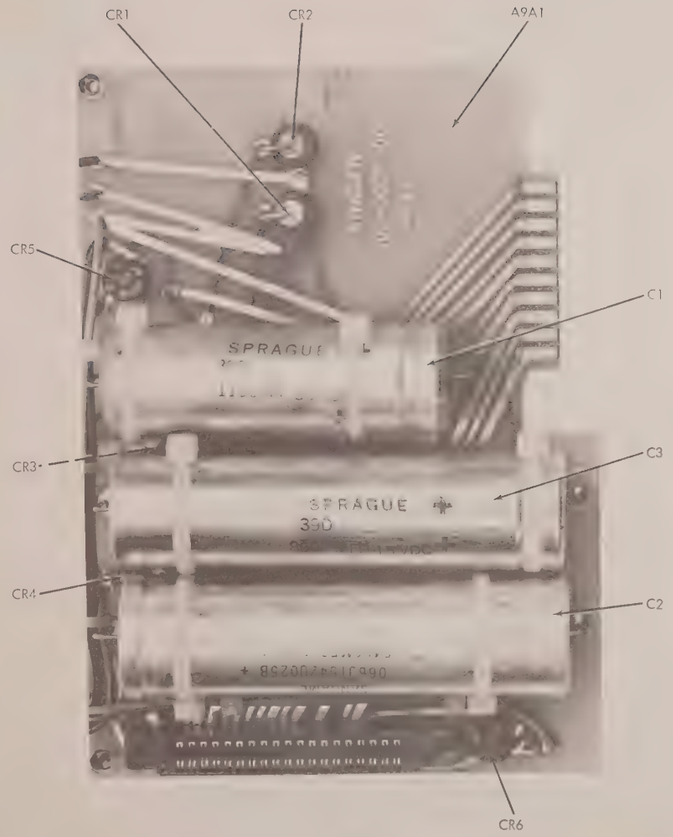
d. Unsolder the two white/blue leads from A5A1A6C1.

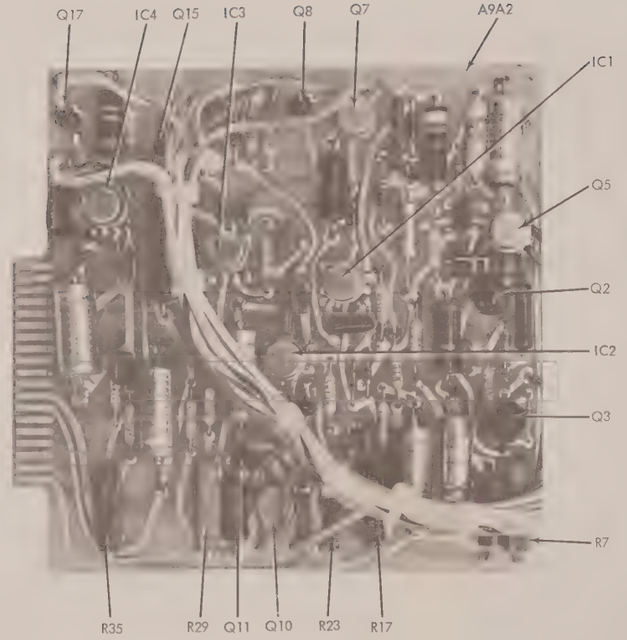
e. Disconnect multipin connector P1 from A5A3J1.

f. Disconnect the following: A4P1 from A5A1J1; P8 from A5A1J3; W1P2 from A5A1J2; A5A5P1 from A6A1AT1J1; and A8P2 from A5A3J2.

g. Remove the four screws loosened in step a and carefully withdraw A5 from the Signal Generator.







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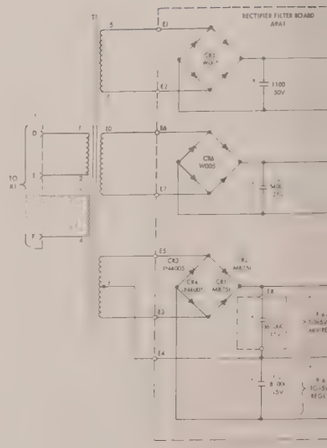
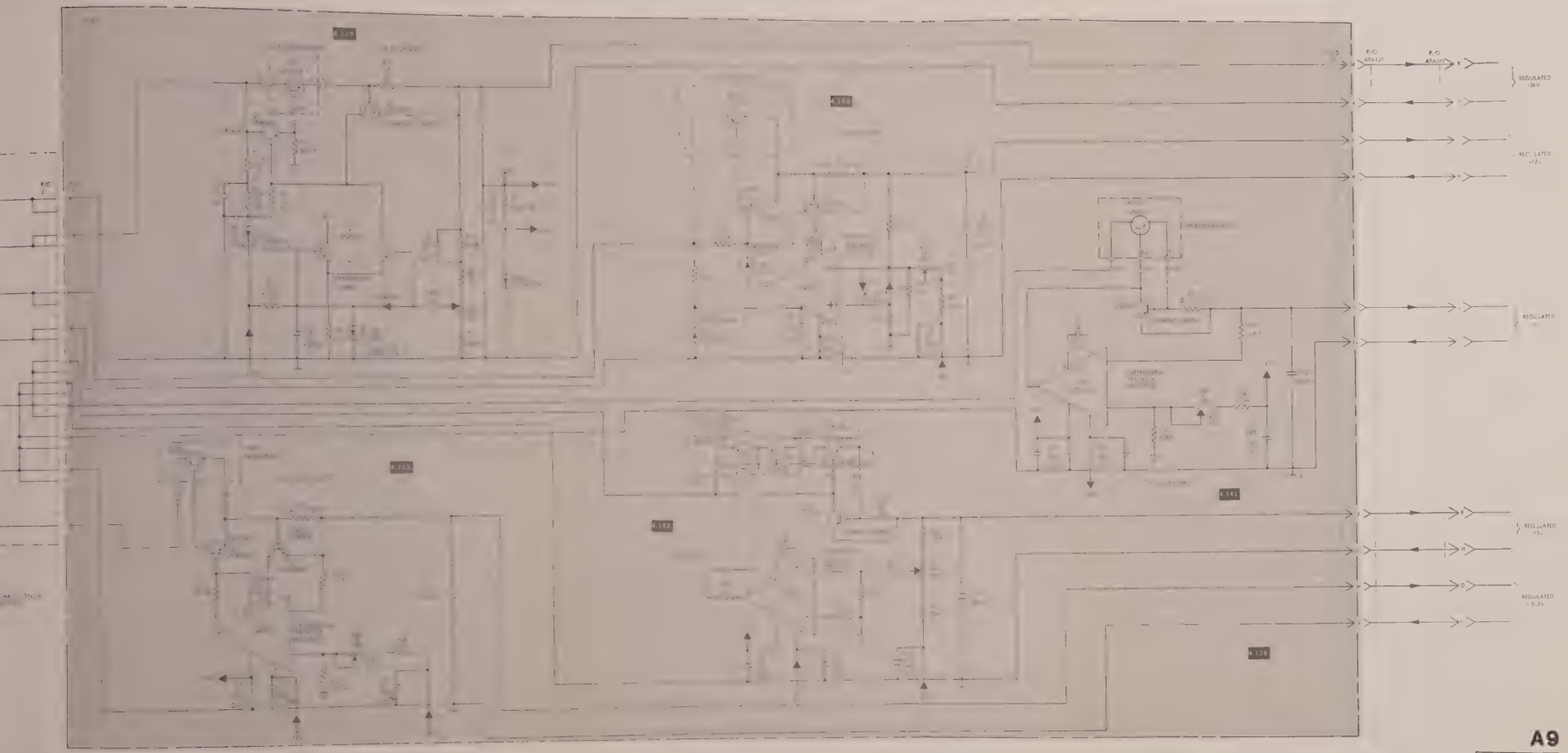
Parts Locations





A9

4 -33.

Figure 4-33. Regulated Power Supplies, Functional Schematic Diagram

4-151. OUTPUT ATTENUATOR A6.

4-152. 0-80 dB Step Attenuator A6A1.

a. Loosen and remove the seven screws that secure the brace to the low-pass filter assembly, main chassis mounting block, and side of plug-in housing. Withdraw the brace from the main chassis.

b. Disconnect A5A5P1 from A6A1AT1J1.

c. Loosen and remove four screws that secure A6A1 to the main chassis bottom plate.

d. Unscrew the coaxial connection which interconnects A6A1 and A6A2.

e. Unsolder the black, white/grey, and blue leads at the GRD and E1 eyelets of A6A1 and the RFI filter, respectively.

f. Carefully withdraw A6A1 from the main chassis.

4-153. 0-70 dB Step Attenuator A6A2.

a. Perform steps a through d of paragraph 4-152.

b. Loosen and remove the four screws that secure A6A2 to the main chassis bottom plate.

c. Unsolder the two coaxial cables from the wiper and end terminals of A6A1R1. Note that one of these cables. terminates at J1-15 and the other at A3C3. Unsolder the remaining coaxial cable from the grounded terminal of A6A1R1. This cable is terminated at P2-P. Unsolder the ground leads of these three cables from the ground lug.

d. Unsolder the blue lead from A6A2 RFI filter. Unsolder the black ground lead from the lug on the filter.

e. Carefully remove A6A2 from the main chassis.

4-154. MODULATION AND SWITCHING ASSEMBLY A7.

a. Remove frequency counter A8 as described in paragraph 4-155.

b. Loosen and remove the five screws that secure A7 to the main chassis bottom plate.

c. Disconnect multipin connector P2 from A7J1.

d. Carefully lift A7 from Signal Generator.

4-155. FREQUENCY COUNTER A8 .

a. Remove the screw that secures the counter box assembly rear support strut to the main chassis bottom plate.

b. Disconnect multipin connector A8P2 from A5A3J2.

c. Disconnect P7, P10 and P11 from A8A1J2, A8A1J4 and A8A1J5, respectively.

d. Disconnect W2P2 and W3P1 from A8A1J3 and A8A1J1, respectively.

e. Remove the two screws that secure the counter box assembly to the upper lip of the front panel.

f. Carefully slide the counter assembly back and withdraw it from the Signal Generator.

4-156. POWER SUPPLY A9.

a. Loosen and remove the four screws that secure the power supply to the main chassis bottom plate.

b. Disconnect snap-on leads from Q1 and Q2 on rear panel of equipment frame. Tag leads to facilitate reassembly.

c. Disconnect AC power multipin connector from A9J1.

d. Carefully lift the assembly from the Signal Generator. To gain access to components on board subassemblies A9A1 and A9A2 (see Figure 4-2), proceed as directed in steps e through h.

e. Remove four screws that secure protective plate (covers A9A1) to assembly A9. Slide plate off A9.

f. Remove two screws which secure A9A1 to assembly A9.

g. Disconnect leads from filter capacitor A9C1 by removing two screws.

h. Lift A9A1 and A9A2 from A9 and remove A9A2 from connector on A9A1.

4-157. VOLTAGE MEASUREMENTS.

4-158. The voltage measurements for the assemblies of the Signal Generator are listed in Tables 4-12 through 4-19. The general conditions for voltage measurements are:

a. All voltages measured with respect to chassis (grd) using VTVM.

b. RANGE MHz and FREQUENCY control set for 8.0 MHz (approximately).

c. Unless other wise specified:

1. All pushbuttons released.

2. All controls set to approximate mid-range.

3. Counter in the normal (unlocked) mode.

d. For full Reference Designator, put Assembly Number in table heading before listed Reference Designator.

TABLE 4-12. VOLTAGE MEASUREMENTS, FREQUENCY DIVIDER, A2

Reference Designation	Transistor Type	Terminal Voltage		
		Emitter	Base	Collector
A1Q1	2N5180	- .7	0	+ 8.6
Q2	A473	- .7	0	+ 8
Q3	2N5133	0	0	+10.4
Q4	2N5183	+10.6	+10.4	+12
Q5	2N5179	- .85	0	+12
A2A1Q1	2N5179	+ 1.7	+ 2.4	+10.2
Q2	2N5179	+ 1.7	+ 2.4	+10.2
Q3	A473	+ 1	- 1.7V	- 9.2
Q4	2N4121	+ 2.6	+ 9.2	+ 9.8
A2A2Q1	5179	+ 1.7	+ 2.4	+10V
Q2	5179	+ 1.7	+ 2.4	+10V
Q3	A473	1	+ 1.7V	+ 9.3V
Q4	2N4121	+ .5V	+ 9.3	+10V
A2A3Q1	A473	- 4.2	- 3.4	- 1.5
A3A1Q1	2N4916	- 2	- 2.5	- 4
A3A2Q1	2N5180	- 4.2	- 3.6	- .7

TABLE 4-13. VOLTAGE MEASUREMENTS, MODULATOR A3

Reference Designation	Transistor Type	Terminal Voltage							
		Emitter		Base			Collector		
A1Q1	2N4275	0		0			.02		
A1Q2	2N4275	- .25		0			+ 7.7		
A1Q3	2N4916	12		11.2			11.		
A1Q4	2N4275	- 4.4		- 3.6			- 4.3		
A1Q5	2N4275	- 4.7		- 4.3			11.8		
A1Q6	2N5468	(S)		(G) 11.4			(D) -1.6		
A1Q7	2N5183	0		.01			6		
A1Q8	2N5183	0		.7			.02		
A1Q9	2N5133	0		.02			12		
A1Q10	2N5460	(S) .005		(G) 11.5			(D) .52		
A1Q11	2N4275	.33		.39			3.04		
A1Q12	2N5179	.25		1			0		
A1Q13	2N4275	0		0			1		
A1Q14	2N4275	0		0			1		
A1Q15	2N5179	.3		1.06			0		
		1	2	3	4	5	6	7	8
MC1		0	.0005	0	-5.2	0	0	12	0
MC2		0	*	0	-5.2	0	0	.502	12
A2A1Q1	2N2857	- .7		0			5.4		
A2A1Q2	2N2857	4.65		5.4			10.8		

* Voltage varies with VERNIER attenuator setting.

TABLE 4-14. VOLTAGE MEASUREMENTS, POWER AMPLIFIER A4

Reference Designation	Transistor Type	Terminal Voltage		
		Emitter	Base	Collector
A1Q1	2N2857	-0.7	0	+ 6
A1Q2	2N2857	+5.2	+6	+11
A1Q3	2N2857	-0.7	+0.02	+ 9.6
A1Q4	2N2857	-0.7	+0.03	+10
A1Q5	2N4427	-1.6	-1	+10.4
A1Q6	2N5109	-0.8	-0.03	+ 9
A1Q7	RE3754	-2.4	-1.7	+12

TABLE 4-15. VOLTAGE MEASUREMENTS, LOW PASS FILTER A5

Reference Designation	Transistor Type	Terminal Voltage		
		Emitter	Base	Collector
A1A2Q1	2N5133	0	0	6
A1A2Q2	2N5183	0	0	5.5V
A1A2Q3	2N5183	0	.5V	.7 VDC

TABLE 4-16. VOLTAGE MEASUREMENTS, ATTENUATOR A6

Reference Designation	Transistor Type	Terminal Voltage*		
		Emitter	Base	Collector
A1A2PT1	FPT100	0	+ .5	+ .15
Q1	2N5133	0	+ .09	+5.3
Q2	2N5133	0	+ .09	+5.3
Q3	2N4916	+6	+5.4	+ .5
Q4	2N5916	+6	+5.4	+ .5
Q5	2N4916	+6	+5.2	+5.9
Q6	2N4916	+6	+5.2	5.9
A2A1PT1	FPT100	0	+ .5	+ .15
PT2	FPT100	0	+ .5	+ .15
PT3	FPT100	0	0	+ .65
Q1	2N5133	0	+ .09	+5.3
Q2	2N5133	0	+ .09	+5.3
Q3	2N5133	0	+ .67	0
Q4	2N4916	+6	+5.4	+ .5
Q5	2N4916	+6	+5.4	+ .5
Q6	2N4916	+6	+5.2	+5.8
Q7	2N4916	+6	+5.2	+5.9
Q8	2N4916	+6	+5.2	5.9
Q9	2N4916	+6	-5.8	0

* All voltages measured with dBm switch set at +10/1.0V position.

TABLE 4-17. VOLTAGE MEASUREMENTS, MODULATION AND SWITCHING ASSEMBLY A7

Reference Designation	Transistor Type	Terminal Voltage							
		Emitter			Base		Collector		
Q1	2N5133	3.23			3.89		7.00		
Q2	2N5460	(S) 0			(G) 3.2		(D) -4.8		
Q3	2N5255	A -.31	B -.27		A -.74	B -.66	A -25.9	B -25.9	
Q4	2N5255	A .264	B .264		A -.31	B -.27	A -25.9	B -25.2	
Q6	2N3645	-25.8			-25.2		-10		
		1	2	3	4	5	6	7	8
A1		-5.2	-.07	0	-5.26	-4.09	11.3	11.9	11.3
A2		-10.5	0	0	-11.8	-10.5	0	11.9	-.52
A3		-10.5	0	0	-11.8	-10.6	0	11.9	-.54
A4		0	0	0	-5.2	3.27	.679	.002	11.97
A5		0	0	0	-5.26	3.33	.517	.16	11.97
A6		0	-.025	-.025	-5.26	3.54	.65	.03	11.97
A7		-3.95	0	0	-5.26	-4.05	.003	11.97	-.52

All measurements made in CW +20 dB

TABLE 4-18. VOLTAGE MEASUREMENTS, FREQUENCY COUNTER A8

Reference Designation	Transistor Type	Terminal Voltage		
		Emitter	Base	Collector
A3A4Q1	2N5134	0	+ 0.6	+ 2
A3A4Q2	2N3904	+ 1.6	+ 2.2	+ 4.7
A3A4Q3	2N3904	+ 0.1	+ 0.8	+ 3.4
A3A4Q4	2N5087	+ 0.8	+ 0.2	0
A3A5Q1	2N5088	+ 0.3	+ 0.9	+ 2.7
A3A5Q2	2N5087	+ 0.8	+ 0.2	0
A3A6Q1	2N5133	+ 1	+ 0.3	+ 3
A3A6Q2	2N5133	+ 2	+ 2.6	+ 2.6
A3A6Q3	2N4916	+ 5	+ 4.1	+ 0.8
A3A6Q4	2N5183	0	+ 0.8	+ 0.02
A3A6Q5	2N5183	+ 0.5	+ 0.9	+ 1.6
A3A6Q6	2N5130	+ 1.8	+ 2	+ 3
A3A7Q1	2N4916	0	+ 2.1	-25.7
A3A7Q2	2N5471	(S) -10.1	(G) -10	(D) -10
A3A7Q3	2N4916	0	+ 2.2	-23.8
A3A7Q4	2N5471	(S) -26	(G) - 0.5	(D) -10.1
A3A7Q5	2N5460	(S) -26	(G) -24.3	(D) -26
A3A7Q6	2N5460	(S) -11.5	(G) -10.3	(D) -26
A3A7Q7	2N4916	0	- 0.7	- 0.05

TABLE 4-19. VOLTAGE MEASUREMENTS, POWER SUPPLY A9

Reference Designation	Transistor Type	Terminal Voltage							
		Emitter		Base			Collector		
Q1	2N4919	-26.9		-26.3			-42.6		
Q2	2N5296	5.8		6.4			8.7		
Q3	2N5296	6.4		7.			9.6		
Q4	2N4901	17.7		16.9			12.5		
Q5	2N3059	-10.5		- 9.8			- 5.8		
A2Q2	2N3638A	- 8.4		-26.9			-27.5		
A2Q3A	2N5255	- 5.6		- 6.3			-26		
A2Q3B	2N5255	- 5.6		- 6.2			-27.5		
A2Q5	2N4030	-26.3		-27.5			-42.6		
A2Q7	2N2219A	12.5		13.1			16.9		
A2Q8	2N5133	12.3		12.5			13.1		
A2Q10	2N4030	- 5.8		- 6.4			- 9.8		
A2Q11	2N5087	- 5.6		- 5.8			- 6.4		
A2Q15	2N5133	5.1		5.3			6.4		
A2Q17	2N5133	6.3		6.4			7		
		1	2	3	4	5	6	7	8
A2IC1		-11.1	.015	.014	-12.3	NC	6.3	11.8	5.7
A2IC2		-10.9	.02	.02	-12.3	NC	6.4	11.8	5.7
A2IC3		-11.2	.02	.02	-12.3	NC	6.6	12.1	6.1
A2IC4		-11.1	6.02	6.02	-12.3	NC	7.0	12.1	6.7
Q1 (Rear Panel)	2N4901	9.4			8.7		5.8		
Q2 (Rear Panel)	2N4901	9.4			8.7		5.8		

4–159. ALIGNMENT AND CALIBRATION.

4-160. The adjustments required for the alignment and calibration of the Signal Generator (exclusive of the power supply and the frequency counter) are located on modulation and switching assembly A7. To gain access to the adjustments on assembly A7, remove the left side panel. The location of the adjustments on A7 are shown in Figure 4-13.

NOTE

Allow the Signal Generator a 30-minute warmup period before performing the alignment and calibration procedures.

4-161. CALIBRATING RF LEVEL METER.

NOTE

Before calibrating the RF LEVEL meter, check that it is mechanically zeroed. If necessary, adjust the pointer mechanical zero positioning screw (located below the meter).

a. Set the front-panel controls as indicated below.

Control	Setting
POWER	Pressed
dBm Selector Switch	+10/1.0V
dBm Vernier Level	Fully Clockwise
VX2	Released
CW	Pressed
AM/FM	AM
EXT COUNT	Released
RANGE MHz	62 - 128
FREQUENCY	100 MHz
VERNIER Frequency	Mid-range
AM LEVEL	Fully Clockwise
FM DEV	Fully Clockwise
Remaining Controls	As Desired

b. Connect a General Microwave 421C/454A thermistor mount/power meter to the RF OUT connector via a calibrated 20 dB, 50Ω pad.

c. Adjust the front-panel dBm vernier level control until the General Microwave 454A power meter indicates -6 dBm (which corresponds to +14 dBm at the RF OUT connector).

d. With the VX2 pushbutton released, adjust RF mtr cal (X1) potentiometer A7R22 for a full-scale reading (+4 dB) on the RF LEVEL meter.

e. Press the VX2 pushbutton and adjust the dBm vernier level control, as necessary, until the General Microwave 454A power meter indicates 0 dBm (which corresponds to +20 dBm at the RF OUT connector).

f. With the VX2 pushbutton pressed, adjust RF mtr cal (X2) potentiometer A7R23 for a full-scale reading (+4 dB) on the RF LEVEL meter.

g. Release the VX2 pushbutton. The RF LEVEL meter should indicate +4 dB. If not, repeat steps c through g.

4-162. CALIBRATING % AM/FM DEV METER.

NOTE

Before calibrating the % AM/FM DEV meter, check that it is mechanically zeroed. If necessary, adjust the pointer mechanical zero positioning screw (located below the meter).

a. Set the front-panel controls as indicated in step a of paragraph 4-161, except set the Signal Generator frequency to 25 MHz.

b. Connect a Tektronix 585 oscilloscope to the RF OUT connector, via a Narda 20 dB pad.

c. Press the AM INT pushbutton, and adjust the AM LEVEL control for a 100% AM display on the oscilloscope (2 or 3 cycle presentation with a peak-to-peak amplitude of 4 cm and a trough-to-trough amplitude of 0 cm).

d. Adjust % AM cal potentiometer A7R14 for a full-scale reading (100% AM) on the % AM/FM DEV meter.

e. Set the Signal Generator frequency to 100 MHz and press the FM EXT pushbutton.

f. Connect a Hewlett-Packare 3450A DC digital voltmeter to test point A7TP3. Adjust FM cal volts potentiometer A7R80 to obtain a digital voltmeter reading of +0.338 volts ±1 millivolt.

g. With the FM EXT pushbutton in the pressed position, press the FM CAL push-to-operate control and while holding it pressed, rotate the control fully ccw. Note the reading on the frequency counter display. Then, carefully adjust the FM CAL control until the frequency counter display reading increases .100. Carefully release the FM CAL control.

h. Couple a Singer Model SA-70 Spectrum Analyzer to the RF OUT connector.

i. Set the AM/FM switch to FM and press the 100 pushbutton of the FM RANGE (kHz) pushbuttons.

j. Couple an H-P 651B test oscillator to the FM connector. Tu the test oscillator to 41.58 kHz (using an Eldorado 1650 counter) and adjust its output level for the first carrier null on the spectrum analyzer.

k. Adjust FM dev mtr cal potentiometer A7R77 for a full-scale reading (100 kHz) on the % AM/FM DEV meter.

4-163. CALIBRATING POWER SUPPLIES AND COUNTER.

4-164. To calibrate Power Supply, see Table 4-2.

4-165. To calibrate Counter, see paragraph 4-42.

SECTION V
PARTS LIST

5-1. INTRODUCTION.

5-2. This parts list section includes all pertinent data necessary to locate, identify, and procure additional parts for the equipment. Parts are listed alphanumerically by reference symbol and include all replaceable electronic items. In some cases, values, ratings and manufacturer sources shown are nominal and variations may be found. Satisfactory replacement may be made with either the listed component or an exact replacement of the part(s) removed from the equipment.

5-3. ORDERING INFORMATION.

5-4. The following instructions will aid in ordering parts from the parts list.

a. Address all inquiries or orders to:

CUSTOMER SERVICE
The Singer Company
3176 Porter Drive
Palo Alto, California 94304

b. Include the following information:

1) Model and Serial Number of instrument.
2) Singer Part Number.
3) Reference Symbol Number.
4) Description (as shown on Parts List).

5-5. HOW TO USE THE PARTS LIST.

5-6. Paragraphs 5-7 through 5-16 describe the use and meaning of the five columns included in the Parts List, Table 5-5. Table 5-1 lists the assemblies covered by the Parts List. Table 5-2 lists the manufacturer's code. Table 5-3 is a list of circuit reference symbols. Table 5-4 is a list of abbreviations used with this Parts List. Table 5-5 is a list of parts used in the Model 6610ED.

5-7 CIRCUIT REFERENCE.

5-8. The Circuit Reference Column contains an alphanumeric listing of parts as they appear on the equipment chassis, illustration, or schematic. The reference designation identifies the parts as to their component function in the instrument.

5-9 DESCRIPTION COLUMN.

5-10. The Description Column contains the identification of component parts, including all pertinent specifications. When the description column is used for a reference symbol for which no part exists, NOT ASSIGNED is placed in the column. In these instances, columns 3, 4, and 5 are left blank.

5-11 SINGER PART NUMBER COLUMN.

5-12. The Singer Part Number column contains the part number as designated by the Singer Company.

5-13 TRUE FSC NUMBER COLUMN.

5-14. The True FSC Number column references the manufacturer by an assigned code number, as listed in Federal Supply Code Handbook H4-2. For manufacturers not listed in the Handbook, a letter code will be assigned. Table 5-2 includes the manufacturer and his code designation.

5-15 TRUE MANUFACTURER'S PART NUMBER COLUMN.

5-16. The True Manufacturer's Part Number shown contains the part number as designated by the manufacturer of the part.

5-17. ACCESSORIES LIST.

5-18. As an aid for ordering mechanical parts which may be worn or lost, the last table in the parts list shows part numbers for the power cord, knobs, pushbuttons and connectors.

5-7 5-9 5-11 5-13 5-15 See Paragraphs Above

Model 6610ED Series

TABLE 5-5. REPLACEABLE PARTS MODEL 6610ED SERIES (CONTINUED)

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A1	(Cont.)			
	RESISTORS			
R54	22.1 kΩ	59-22.1K	19701	MF5C-D-2212F
R55	10.0 kΩ	59-10.0K	19701	MF5C-D-1002F
R56	Factory Selected			
R57	4.02 kΩ	59-4.02K	19701	MF5C-D-4021F

TABLE 5-1. LIST OF ASSEMBLIES

A0	Basic Assembly	A6	Attenuator Assembly
A1	Oscillator	A7	Switch and Modulator
A2	Frequency Divider	A8	Counter Assembly
A3	Modulator	A9	Power Assembly
A4	Power Amplifier 6201	A10	Load Simulator
A5	Low Pass Filter		

TABLE 5-2. FEDERAL SUPPLY CODE FOR MANUFACTURERS

FMC No.	Name and Address of Vendor
00656	Aerovox Corp.; 740 Belleville Ave.; New Bedford, Mass.
01121	Allen Bradley Co.; 1201 South 2nd Street; Milwaukee, Wisconsin 53024
01295	Texas Instruments, Inc; Semi-Conductor Division; 13500 North Central Expressway; Dallas, Texas 75231
02114	Ferroxcube Corp of America; Mt. Marion Road; Saugerties, New York 12477
03782	Singer Instrumentation; 3176 Porter Drive; Palo Alto, California 94304
04099	CAP Capacitors Inc.; P.O. Box 1103, Lubbock, Texas 79408
04713	Motorola Semiconductor Products, Inc.; 5005 East McDowell Road; Phoenix, Arizona 85008
06751	Nuclear Corp of America, Inc; U.S. Semcor Division; Phoenix, Arizona
07263	Fairchild Camera and Instrument Corp.; Semi-Conductor Division; 313 Frontage Road; Mountain View, California
08730	Vemaline Products Co.; 511 Commerce Street; Franklin Lakes, New Jersey 07417
10133	Buss Machine Works Inc.; 8th and Eldon Streets; Holland, Mich.
12617	Hamlin Inc.; Grove and Lake Streets; Lake Mills, Wisconsin 53551
12987	Adelphi Electronics Inc; Jericho Turnpike Westbury; Long Island, New York
14655	Cornell-Dublier Electric Corp.; 50 Paris Street, Newark, New Jersey
18324	Signetics Corp.; 811 East Argues Ave; Sunnyvale, California 94086
18489	Reliable Capacitor Co.; 14716 Arminta Street; Van Nuys, California 91402
19396	Illinois Tool Works Inc; Paktron Division; Alexandria, Virginia
19701	Electra Manufacturing Co; 800 North 21st; Independence, Kansas
23223	CTS Micro Electronics Inc; P.O. Box 1278; West Lafayette, Indiana
23880	Standford Applied Engineering, 340 Morton Ave; Santa Clara, California
25088	Siemens America Inc; 350 Fifth Avenue; New York, New York
27014	National Semi-Conductor Corp; 2950 San Ysidro Way; Santa Clara, California 95051
28363	Corning Glass Works, Technical Products Division, Chestnut Street Division; Corning, New York
28480	Hewlett Packard Co; 1501 Page Mill Road; Palo Alto, California 94304
29750	Satallite Engineering and Sales Co., 7358 Radford Ave; North Hollywood, California 91605
32464	Spectrum Technology Inc; P.O. Box 368, Building 240; Santa Barbara Airport; Goleta, California
33095	Spectrum Control, Inc; 152 East Main Street; Fairview, Pennsylvania 16415
36196	Stanwyck Coil Products Ltd; Hawesbury; Ontario, Canada
53021	Sangamo Electric Co; 1301 North 11th; Springfield, Illinois 62705
56289	Sprague Electric Co; Marshall Street; North Adams, Massachusetts 01247
70371	American Lava Corp.; 219 Kruesi Building; Chattanooga, Tenn.
71590	Centralab Division of Globe-Union Inc; 932 E. Keefe Ave.; Milwaukee, Wisconsin 53212
71744	Chicago Miniature Lamp Works; 4433 Ravenswood Ave.; Chicago, Illinois 60640
72136	Electro Motive Mfg. Co, Inc; The South Park and John Streets; Willimantic, Conn. 06226
72982	Erie Technological Products Inc; 644 W. 12th Street; Erie, Pennsylvania 16512
73138	Helipot, Division of Beckman Instruments Inc; Fullerton, California
73445	Amperex Electronic Co, Division of North American Phillips Co., Inc; Hicksville, New York
75042	IRC, Inc; 401 North Broad Street; Philadelphia, Pennsylvania 19108
75292	Kingwell Bros. Ltd; 457 Minna; San Francisco, California 94101
77638	General Instrument Corp.; Rectifier Division; 240 Wythe Ave.; Brooklyn, New York
84411	TRW, Capacitor Division; Ogallala, Washington
85514	Brownell Distributors Inc; 85-10th Ave.; New York, New York
88245	Litton Industries, Useco Division; 13536 Saticoy Street; Van Nuys, California
90201	Mallory Capacitor Co.; 3029 East Washington Street; P.O. Box 372; Indianapolis, Indiana 46206
93702	Cutter Laboratories; Fourth and Parker Streets; Berekely, California
95238	Continental Connector Corp.; Woodside, New York
98291	Sealectro Corp; 225 Hoyt; Mamaroneck, New York
99848	Wilco Corp.; 4030 W. 10th Street, P.O. Box 22248; Indianapolis, Indiana 46222

TABLE 5-3. REFERENCE SYMBOLS

AT	Attenuator, Isolator	OI	Optical Isolator
C	Capacitor	P	Plug, Connector
CR	Diode	Q	Transistor
CD	Directional Coupler	R	Resistor
DS	Lamp	S	Switch
J	Jack, Connector	T	Transformer
K	Relay	U	Integrated Circuit
L	Inductor	Z	Miscellaneous Parts: Ferrite Beads (RF Choke)

TABLE 5-4. ABBREVIATIONS

AF	Audio Frequency, 30 Hz - 30 kHz	mV	Millivolts
Cer.	Ceramic	mW	Milliwatts
Comp.	Composition	No.	Number
Dep. Car.	Deposited Carbon	NPNT	N Pole N Throw (N=Digit)(S=Single)
DM	Dipped Mica	Oper. Ampl.	Operational Amplifier
Elec.	Electrolytic, Aluminum	P/O	Part of
EHF	Extremely High Frequency, 30 - 300 GHz	Pot.	Potentiometer
F	Frequency	pF	Picofarad
Fact. Sel.	Factory Selected	RF	Radio Frequency
Freq. Mul	Frequency Multiplier	Rect.	Rectifier
GMV	Guaranteed Minimum Value	SAF	Sub Audio Frequency, 0 - 30 Hz
GP	General Purpose	SHF	Super High Frequency, 3.0 - 30 GHz
HC	Hot Carrier (Diode)	Spec.	Special
HF	High Frequency, 3 - 30 MHz	Tant.	Tantalum, Electrolytic
IND-STD	Industry Standard	UHF	Ultra High Frequency, 300 - 3000 MHz (0.3 - 3.0 GHz)
k	Thousand	V	Volts
LED	Light Emitting Diode	Var.	Variable
LF	Low Frequency, 30 - 300 kHz	VHF	Very High Frequency, 30 - 300 MHz
m	0.001 (1/1000)	W	Watts
M	Million	WW	Wirewound
mA	Milliamperes	0 TC	Zero Temperature Coefficient
MF	Metal Film	%	± % if sign not shown
Med. Freq.	Medium Frequency, 300 - 3000 kHz	Ω	Ohms
Mfr.	Manufacturer	µF	Microfarads

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
	NOTE: Each assembly reference is to be prefaced by A1. Each circuit element reference is to be prefaced by its assembly number, for a total description.			
A0	BASIC ASSEMBLY	101-0452-003	03782	101-0452-003
A0A1	DIVIDER/MODULATOR	103-1966-003	03782	103-1966-003
A0A1A1	PLATE & FILTER	103-1968-001	03782	103-1968-001
A0A1A1A1	FILTER	103-1967-001	03782	103-1967-001
	CAPACITORS			
	NOTE: Unless otherwise specified, all capacitors are fixed ceramic.			
C1, C2	2500 pF, GMV, 500 V FT	150-1011-001	00656	BSF-1CC/252Z
C3, C4	1000 pF, GMV, 500 V FT	556-005-381	01121	FA5C/102W
C5, C6	2500 pF, GMV, 500 V FT	150-1011-001	00656	BSF-1CC/252Z
	INDUCTORS			
L1 thru L4	Choke 750 Ω/50 MHz, ±20%	156-7005-002	02114	VK200 10/3B
A0A2	CASE ASSY.	103-3104-001	03782	103-3104-001
	TRANSISTORS			
Q1, Q2	40 VC Max, 87.5 W, B20-80	153-0018-001	IND-STD	2N4901
	SWITCHES			
S2, S6	Slide Switch Modified	913-919	03782	913-919
A1	OSCILLATOR	103-3097-002	03782	103-3097-002
	CAPACITORS			
C1, C2	Fixed, Cer., 2500 pF, GMV, 500 V FT	150-1011-001	00656	BSF-1CC/252Z
	INDUCTOR			
L1	Choke 750 Ω/50 MHz, ± 20%	156-7005-002	02114	VK200 10/3B
A1A1	OSCILLATOR	103-1844-001	03782	103-1844-001
	CAPACITORS			
C1	Fixed, Cer., 470 pF, ± 10%, 100V	150-7001-001	70371	CM310-501
C2	Fixed, Cer., .01 μ F, ± 10%, 200 V	150-1014-103	70371	CM-1712
C3	Fixed, Cer., 2 μ F, ± .25 pF, 500 V	556-060-166	72982	CC20CK020C
	INDUCTOR			
L1	2 1/2 Turns on 1/2 W Res., 10 M Ω, #18 Wire	132-0380-009	03782	132-0380-009
	RESISTORS			
R1	Comp, 330 Ω, ± 5%, 1/2 W	151-1003-331J	19701	CR37-1-2-5P-330Ω
R2	Comp, 2400 Ω, ± 5%, 1/4 W	151-1002-242J	19701	CR25-1-4-5P-2.4K

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A1A1	(Cont.)			
R3	Comp, 3300Ω, ±5%, 1/4 W	151-1002-332J	19701	CR25-1-4-P5-3.3K
R4	Comp, 470Ω, ±5%, 1/4 W	151-1002-471J	19701	CR25-1-4-P5-470Ω
	TRANSISTOR			
Q1	30 VC Max, 5.0 W, B10-200	81-154	IND-STD	2N3866
A1A2	CENTER CONDUCTOR	103-3096-001	03782	103-3096-001
A1A2A1	END CAP	103-3095-001	03782	103-3095-001
	CAPACITORS			
C3, C4	FT Modified, 100 pF, ± 20%, 500 V	149-0239-001	03782	149-0239-001
	DIODE			
CR1	Varactor, 33 pF @ 4 V, 60 VC Max	154-5001-001	IND-STD	IN5146
	INDUCTOR			
L1	Toroid Core	556-146-999	02114	5659065/3B
	RESISTOR			
R1	Fixed Comp, 3.3 K, ± 5%, 1/8 W	32-3.3 K	19701	CR16-1-8-5P-3.3K
A2	FREQUENCY DIVIDER	103-1959-002	03782	103-1959-002
	INDUCTOR			
L1	7 Turns, #32 Wire, Ferrite Core	132-0377-001	03782	132-0377-001
A2A1	BAND SWITCH	103-1961-003	03782	103-1961-003
A2A1A1	FREQ BIV BAND SWITCH	103-1827-003	03782	103-1827-003
	CAPACITORS			
	NOTE: Unless otherwise specified, all capacitors are fixed ceramic.			
C1	1 pF, ±.25 pF, 500 V	150-1012-010CC	75292	CC20CK010C
C2, C3	.001 µF, ±10%, 1000V	556-060-046	71590	DD-102
C4	6 pF, ±.25 pF, 500 V	150-1012-060	75292	CC20CH060C
C5	2 µF, ±.25 pF, 500V	556-060-166	72982	CC20CK020C
C6	0.01 µ F, ± 20 %, 25 V	12-56	71590	UK25-103
C7 thru C9	.001 µF, ±10%, 1000 V	556-060-046	71590	DD-102
C10	15 pF, ±5%, 500 V	150-2002-150CJO	72136	DM15C150J0500
C11 thru C13	.001 µF, ±10%, 1000 V	556-060-046	71590	DD-102
C14	.01 µF, ±10%, 200 V	150-1014-103	70371	CM-1712

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A2A1A1	(Cont.)			
C15 thru C17	.001 µF, ±10%, 1000 V	556-060-046	71590	DD-102
C18	.01 µF, ±10%, 200 V	150-1014-103	70371	CM-1712
C19	180 pF, ±2%, 500 V DM	150-2002-181FG0	72136	CD15FD181G03
C20	270 pF, ±2%, 500 V DM	150-2002-271FG0	72136	DM15F271G0
	INDUCTORS			
L1	3 Turns #22 Wire On 10 MΩ, 1/2 W Comp Res	132-0380-003	03782	132-0380-003
L2	NOT ASSIGNED			
L3	3 Turns, #26 Wire On 2.7 MΩ, 1/4 W Comp Res	132-0383-003	03782	132-0383-003
L4	NOT ASSIGNED			
L5, L6	7 Turns, #32 Wire Ferrite Core	132-0377-001	03782	132-0377-001
	TRANSISTORS			
Q1	12 VC Max, 200 mW, B25-250	153-3005-001	IND-STD	2N5179
Q2	VHF, NPN, Silicon, 40 VC Max, 260 mW	153-3002-001	73445	A473
Q3	NPN, Silicon, 20 VC Max, 500 mW, B60-1000	153-3009-001	IND-STD	2N5133
Q4	NPN, Silicon, 18 VC Max, 500 mW, B75-min.	153-3003-001	IND-STD	2N5183
Q5	20 VC Max, 200 mW	153-3005-001	IND-STD	2N5179
	RESISTORS			
	NOTE: Unless otherwise specified, all resistors are fixed comp. 1/4 W, ±5%.			
R1	75Ω	151-1002-750J	19701	CR25-1-4-5P-75Ω
R2	620Ω	151-1002-621J	19701	CR25-1-4-5P-620Ω
R3	510Ω	151-1002-511J	19701	CR25-1-4-5P-510Ω
R4	300Ω	151-1002-301J	19701	CR25-1-4-5P-300Ω
R5, R6	47Ω	151-1002-470J	19701	CR25-1-4-5P-47Ω
R7	300Ω	151-1002-301J	19701	CR37-1-2-5P-330Ω
R8	10KΩ	151-1002-103J	19701	CR25-1-4-5P-10K
R9	47Ω	151-1002-470J	19701	CR25-1-4-5P-47Ω
R10	100Ω	151-1002-101J	19701	CR25-1-4-5P-100Ω
R11	330Ω	151-1002-331J	19701	CR37-1-2-5P-330Ω

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A2A1A1	(Cont.)			
R12	47Ω	151-1002-470J	19701	CR25-1-4-5P-47Ω
R13	330Ω	151-1002-331J	19701	CR25-1-4-5P-330Ω
R14	NOT ASSIGNED			
R15	10Ω	151-1002-100J	19701	CR25-1-4-5P-10Ω
R16	330Ω	151-1002-331J	19701	CR25-1-4-5P-300Ω
R17, R18	150Ω	151-1002-151J	19701	CR25-1-4-5P-150Ω
R19	820Ω	151-1002-821J	19701	CR25-1-4-5P-820Ω
R20	10.0kΩ, ±1%, MF	59-10.0K	19701	RN55-D-1002F
	TRANSFORMER			
T1	50/12.5Ω	132-0277-001	03782	132-0277-001
A2A2	BOX	103-1963-001	03782	103-1963-001
	CAPACITORS			
C1	NOT ASSIGNED			
C2 thru C4	1000 pF, ±10% FT	556-146-746	72982	2404-000-X5UO-102P
C5	NOT ASSIGNED			
C6	NOT ASSIGNED			
C7	1000 pF, ±10% FT	556-146-746	72982	2404-000-X5UO-102P
C8	Fixed, Cer., 1000 pF, GMV, 500 V	556-074-124	32464	SS5D-102W/14-6447
	FILTERS			
FL1 thru FL3	500 pF, 10A Max, 200 W	556-146-774	72982	1270-016
	INDUCTORS			
L1 thru L3	7 Turns, #32 Wire, Ferrite Core	132-0377-001	03782	132-0377-001
	RESISTORS			
	NOTE: Unless otherwise specified, all resistors are fixed comp., 1/4W, ±5%.			
R1, R2	1 KΩ	151-1002-102J	19701	CR25-1-4-5P-1K
R3	100Ω	151-1002-101J	19701	CR25-1-4-5P-100Ω
R4	220Ω	151-1002-221J	19701	CR25-1-4-5P-220Ω
R5	1 KΩ	151-1002-102J	19701	CR25-1-4-5P-1K

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A2A2A1	FREQ DIV. 2	103-1883-001	03782	103-1883-001
	CAPACITORS			
	NOTE: Unless otherwise stated, all capacitors are fixed ceramic.			
C1	15 pF, ±5%, 500 V, DM	150-2002-150CJ0	72136	DM15C150J0500
C2	10 pF, ±5%, 500 V, DM	150-2002-100CJ0	IND-STD	CM06CD100J03
C3	15 pF, ±5%, 500 V, DM	150-2002-150CJ0	72136	DM15C150J0500
C4	56 pF, ±10%, 1000 V	150-1018-560	71590	DD-560
C5	68 pF, ±10%, 200 V	12-59	00656	CK05BX680K
C6	.001 µF, ±10%, 1000 V	556-060-046	71590	DD-102
C7	6.8 pF, ±10%, 1000 V	150-101806R8	71590	DD6R8
C8	.001 µF, ±10%, 1000 V	556-060-046	71590	DD-102
C9	6.8 pF, ±.5%, 200V	150-1017-6R8	72982	8111-026-C0G0689D
C10	68 pF, ±10%, 200V	12-59	00656	CK05BX680K
C11	.001 µF, ±10%, 1000 V	556-060-046	71590	DD-102
C12	0.01 µF, ±20 %, 25 V	12-56	71590	JK25-103
C13	6 pF, ±0.25 pF, 500 V	150-1012-060CC	75292	CC20CH060C
C14	39 pF, ±2%, 500 V	150-2002-390EG0	72136	CD15ED390G03
C15	33 pF, ±2%, 500 V DM	150-2002-330EG0	14655	CD15ED330G03
	DIODES			
CR1	Switching, Silicon, 25 V, 4.0 nS Recovery	556-146-880	07263	FDH-666
CR2, CR3	Selected Pair, V_F same ±5mV at 0.1 mA and 1.0mA	134-0059-001	03782	132-0059-001
	INDUCTORS			
L1	5 Turns, #26 Wire on 2.7 MΩ, 1/4 W Comp Res	132-0383-005	03782	132-0383-005
L2	7 Turns, #32 Wire Ferrite Core	132-0377-001	03782	132-0377-001
L3	6 Turns, #26 Wire on 2.7 MΩ, 1/4 W Comp Res	132-0383-006	03782	132-0383-006
	TRANSISTORS			
Q1, Q2	Matched Set, 12 VC Max, 200 mW, B25-250	134-0060-001	IND-STD	2N5179
Q3	VHF, NPN, Silicon, 40 VC Max, 260 mW, B27-min.	153-3002-001	73445	A473

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A2A2A1	(Cont.)			
Q4	PNP, 30 VC Max, 500 mW, B150-300	81-189	07263	2N4917
	RESISTORS			
	NOTE: Unless otherwise specified, all resistors are fixed comp. 1/4W, ±5%.			
R1	1KΩ	151-1002-102J	19701	CR25-1-4-5P-1K
R2	91Ω	151-1002-910J	19701	CR25-1-4-5P-91Ω
R3	150Ω	151-1002-151J	19701	CR25-1-4-5P-150Ω
R4	300Ω	151-1002-301J	19701	CR25-1-4-5P-300Ω
R5	2KΩ, 1/8 W	151-1016-202J	19701	CR16-1-8-5P-2K
R6	330Ω	151-1002-331J	19701	CR37-1-2-5P-330Ω
R7	2KΩ, 1/8 W	151-1016-202J	19701	CR25-1-4-5P-2K
R8	150Ω	151-1002-151J	19701	CR25-1-4-5P-150Ω
R9	300Ω	151-1002-301J	19701	CR25-1-4-5P-300Ω
R10	120Ω	151-1002-121J	19701	CR25-1-4-5P-120Ω
R11	10Ω	151-1002-100J	19701	CR25-1-4-5P-10Ω
R12	5600Ω	151-1002-562J	19701	CR25-1-4-5P-5.6K
R13	1KΩ	151-1002-102J	19701	CR25-1-4-5P-1K
R14	220Ω	151-1002-221J	19701	CR25-1-4-5P-220Ω
R15	560Ω	151-1002-561J	19701	CR25-1-4-5P-560Ω
R16	150Ω	151-1002-151J	19701	CR25-1-4-5P-150Ω
R17	200Ω	151-1002-201J	19701	CR25-1-4-5P-200Ω
R18	100Ω	151-1002-101J	19701	CR25-1-4-5P-100Ω
R19	200Ω	151-1002-201J	19701	CR25-1-4-5P-200Ω
A2A2A2	FREQ DIV. 3	103-1883-002	03782	103-1883-002
	CAPACITORS			
	NOTE: Unless otherwise stated, all capacitors are fixed ceramic.			
C1	100 pF, ±2%, 500 V DM	150-2002-101FG0	14655	CD15FD101G03
C2	43 pF, ±2%, 500 V DM	150-2002-430EG0	72136	DM15E430G0
C3	100 pF, ±2%, 500 V DM	150-2002-220EG0	72136	DM15E220G0

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A2A2A2	(Cont.)			
C4	43 pF, ±2%, 500 V DM	150-2002-430EG0	72136	DM15E430G0
C5	75 pF, ±2%, 500 V DM	150-2002-750EG0	34593	CD15ED750G03
C6, C7	.001 µF, ±10%, 1000 V	556-060-046	71590	DD-102
C8	6.8 pF, ±10%, 1000 V	150-1018-6R8	71590	DD6R8
C9	6.8 pF, ±.5%, 200 V	150-1017-6R8	72982	8111-026-C0G0689D
C10	.001 µF, ±10%, 1000 V	556-060-046	71590	DD-102
C11	75 pF, ±2%, 500 V DM	150-2002-750EG0	34593	CD15ED750G03
C12	100 PF, ±2%, 500 V DM	150-2002-101FG0	14655	CD15FD101G03
C13	.01 µF, +60-40%, 250 V	556-060-146	71590	DDM103
C14	7 pF, ±.25%, 500 V	150-1012-070CC	75292	CC20CH070C
C15	68 pF, ±2%, 500 V DM	150-2002-680EG0	34593	CD15ED680G03
C16	100 pF, ±2%, 500 V DM	150-2002-101FG0	14655	CD15FD101G03
	DIODES			
CR1	Switching, Silicon, 25 V, 4.0 nS Recovery	556-146-880	07253	FDH-666
CR2, CR3	Selected Pair, V_F same ±5mV at 0.1 mA and 1.0 mA	134-0059-001	03782	134-0059-001
	INDUCTORS			
L1	6 Turns, #26 Wire on 2.7 MΩ, 1/4 W comp. res	132-0383-006	03782	132-0383-006
L2	7 Turns, #32 Wire Ferrite Core			
	TRANSISTORS			
Q1, Q2	FB Matched Set, 12 VC Max, 200 MW B25-250	134-0060-001	IND-STD	2N5179
Q3	VHF, NPN, Silicon, 40 VC Max, 260 MW B27-min.	153-3002-001	73445	A473
Q4	PNP Silicon Hi-Speed Sw & RF Amp, 40 VC Max, 200 MW B70-min.	153-3014-001	IND-STD	2N4121
	RESISTORS			
	NOTE: Unless otherwise specified, all resistors are fixed comp. 1/4 W, ±5%.			
R1	1KΩ	151-1002-102J	19701	CR25-1-4-5P-1K
R2	220Ω	151-1002-221J	19701	CR25-1-4-5P-220Ω
R3	150Ω	151-1002-151J	19701	CR25-1-4-5P-150Ω

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A2A2A2	(Cont.)			
R3, R4	150Ω	151-1002-151J	19701	CR25-1-4-5P-150Ω
R5	300Ω	151-1002-301J	19701	CR25-1-4-5P-300Ω
R6	2KΩ, 1/8 W	151-1016-202J	19701	CR25-1-4-5P-2K
R7	330Ω	151-1002-562J	19701	CR25-1-4-5P-5.6K
R8	2KΩ, 1/8 W	151-1016-202J	19701	CR25-1-4-5P-2K
R9	150Ω	151-1002-151J	19701	CR25-1-4-5P-150Ω
R10	300Ω	151-1002-301J	19701	CR25-1-4-5P-300Ω
R11	150Ω	151-1002-151J	19701	CR25-1-4-5P-150Ω
R12	10Ω	151-1002-100J	19701	CR25-1-4-5P-10Ω
R13	5600Ω	151-1002-562J	19701	CR25-1-4-5P-5.6K
R14	1KΩ	151-1002-102J	19701	CR25-1-4-5P-1K
R15	220Ω	151-1002-221J	19701	CR25-1-4-5P-220Ω
R16	560Ω	151-1002-561J	19701	CR25-1-4-5P-560Ω
R17	150Ω	151-1002-151J	19701	CR25-1-4-5P-150Ω
R18	43Ω	151-1002-430J	19701	CR25-1-4-5P-43Ω
R19	100Ω	151-1002-101J	19701	CR25-1-4-5P-100Ω
A2A2A3	FREQ DIV. 4	103-1884-001	03782	103-1884-001
	CAPACITORS			
C1 thru C8	.01 μF, ±10%, 150 V, Cer.	150-1034-001	72982	8141-M100-C0G-103K
	INDUCTORS			
L1	7 Turns, #32 Wire Ferrite Core	132-0377-001	03782	132-0377-001
	INTEGRATED CIRCUIT			
MC1	Flip-Flop, Dual In-Line	153-7013-001	04713	MC1034P
	TRANSISTOR			
Q1	VHF, NPN, Silicon, 40 VC Max, 260 MW B27-min.	153-3002-001	73445	A473
	RESISTORS			
	NOTE: Unless otherwise specified, all resistors are fixed comp. 1/4W, ±5%.			
R1	24K	151-1002-243J	19701	CR25-1-4-5P-24K

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A2A2A3	(Cont.)			
R2	240Ω	151-1002-241J	19701	CR25-1-4-5P-240Ω
R3	47Ω	151-1002-470J	19701	CR25-1-4-5P-47Ω
R4	100Ω	151-1002-101J	19701	CR25-1-4-5P-100Ω
R5	200Ω	151-1002-201J	19701	CR25-1-4-5P-200Ω
R6	3.6 K	151-1002-362J	19701	CR25-1-4-5P-3.6K
R7	1.5 KΩ	151-1002-152J	19701	CR25-1-4-5P-1.5K
R8	470 Ω	151-1002-471J	19701	CR25-1-4-5P-470Ω
R9	5.1 KΩ	151-1002-512J	19701	CR25-1-4-5P-5.1K
A2A3	DIVIDER	103-1962-001	03782	103-1962-001
	FILTERS			
FL1, FL2	500 pF, 200 V, 10 A Max	556-146-774	72982	1270-016
	INDUCTORS			
L1, L2	7 Turns, #32 Wire Ferrite Core	132-0377-001	03782	132-0377-001
A2A3A1	FREQ DIV. 5	103-1945-001	03782	103-1945-001
	CAPACITORS			
C1 thru C4	0.01 µF, ±20%, 25 V, fixed cer.	12-56	71590	UK25-103
C5	33 pF, ±10%, 100 V, fixed cer.	150-1017-330	72982	8121-100-C0G0-330K
	DIODE			
CR1	Switching, MF, 10 mA, 75V	154-3001-001	IND-STD	IN4454
	INTEGRATED CIRCUIT			
MC1	AC Coupled Flip-Flop, 85 MHz	153-7003-001	04713	MC1013P
	TRANSISTOR			
Q1	Difused Silicon Planar, 30 VC Max, 500 MW, B150-300	556-147-059	IND-STD	2N4916
	RESISTORS			
	NOTE: Unless otherwise specified, all resistors are fixed comp. 1/4 W, ±5%.			
R1	5.1 KΩ	151-1002-512J	19701	CR25-1-4-5P-5.1K
R2	1.8 KΩ	151-1002-182J	19701	CR25-1-4-5P-1.8K
R3	330Ω	151-1002-331J	19701	CR25-1-4-5P-330Ω

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A2A3A1	(Cont.)			
R4	150Ω	151-1002-151J	19701	CR25-1-4-5P-150Ω
R5	750Ω, 1/8 W	151-1016-751J	19701	CR16-1-8-5P-750Ω
R6	1 KΩ	151-1002-102J	19701	CR25-1-4-5P-1K
R7	1.2 KΩ	151-1002-122J	19701	CR25-1-4-5P-1.2K
R8	6.2 K	151-1002-622J	19701	CR25-1-4-5P-6.2K
R9, R10	20 KΩ	151-1002-203J	19701	CR25-1-4-5P-20K
R11	1.5 KΩ	151-1002-152J	19701	CR25-1-4-5P-1.5K
A2A3A2	FREQ DIV. 6	103-1946-001	03782	103-1946-001
	CAPACITORS			
C1 thru C6	0.01 μF, ±20%, 25 V, fixed cer.	12-56	71590	UK25-103
	INDUCTOR			
L1	7 Turns, #32 Wire Ferrite Core	132-0377-001	03782	132-0377-001
	INTEGRATED CIRCUIT			
MC1	AC Coupled Flip-Flop, 85 MHz	153-7003-001	04713	MC1013P
	TRANSISTOR			
Q1	20 VC Max, 200 mW, B25-250	153-3005-001	IND-STD	2N5179
	RESISTORS			
	NOTE: Unless otherwise specified, all resistors are fixed comp. 1/4 W, ±5%.			
R1 thru R3	1.8 KΩ	151-1002-182J	19701	CR25-1-4-5P-1.8K
R4	180 Ω	151-1002-181J	19701	CR25-1-4-5P-180Ω
R5	3300 Ω	151-1002-332J	19701	CR25-1-4-5P-3.3K
R6	240 Ω	151-1002-241J	19701	CR25-1-4-5P-240Ω
R7, R8	100 Ω	151-1002-101J	19701	CR25-1-4-5P-100Ω
A3	MODULATOR	103-1958-002	03782	103-1958-002
	CAPACITORS			
C1, C2	2500 pF, GMV, 500 V, FT	150-1011-001	00656	BSF-ICC/252Z
C3	NOT ASSIGNED			
C4	100 pF, GMV, 500 V, FT	150-1011-002	00656	BSF-ICC/101M

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A3A1	PCA COMP/MOD/DRIVER	103-1843-002	03782	103-1843-002
	CAPACITORS			
	NOTE: Unless otherwise stated, all capacitors are fixed mica.			
C1	.1 µF, ±20%, 25 V, fixed cer.	556-120-162	56289	5C023104X0250B3
C2	0.01 µF, ±20%, 25 V, fixed cer.	12-56	71590	UK25-103
C3	.1 µF, ±20%, 25 V, fixed cer.	556-120-162	56289	5C023104X0250B3
C4	8 pF, ±.25 pF, 500 V	150-1012-080CC	75292	CC20CH080C
C5	50 µF, 50 V Elec.	150-5001-500DS	56289	30D506G050DD2
C6, C7	.1 µF, ±20%, 25 V, fixed cer.	556-120-162	56289	5C023104X0250B3
C8, C9	0.01 µF, ±20%, 25 V, fixed cer.	12-56	71590	UK25-103
C10	160 pF, ±2%, 500 V	150-2002-161FG0	72136	DM15F161G0500
C11	5 µF, +75-10%, 6 V, Elec.	150-5001-5R0BS	04099	NLW5-16
C12	43 pF, ±2%, 500 V	150-2002-430EG0	72136	DM15E430G0
C13, C14	.1 µF, ±20%, 25 V, fixed cer.	556-120-162	56289	5C023104X0250B3
C15	Factory Selected			
C16	100 pF, ±2%, 500 V	150-2002-101FG0	14655	CD15FD101G03
C17	.047 µF, ±10%, 50 V, PL	150-1021-001	19396	MY400
C18	.1 µF, ±20%, 25 V, fixed cer.	556-120-162	56289	5C023104X0250B3
C19	51 pF, ±2%, 500 V, Elec. Mica	150-2002-510EG0	72136	CD15ED510G03
C20	.0.01 µF, ±20%, 25 V, fixed cer.	12-56	71590	UK25-103
C21	.1 µF, ±20%, 25 V, fixed cer.	556-120-162	56289	5C023104X0250B3
C22	.0047 µF, ±20%, 50 V, PL	150-4002-J472M	84411	601PE/.0047/20%
C23	.1 µF, ±20%, 25 V, fixed cer.	556-120-162	56289	5C023104X0250B3
C24	0.01 µF, ±20%, 25 V, fixed cer.	12-56	71590	UK25-103
	DIODES			
CR1, CR2	Switching, MF, 10 mA, 75 V	154-3001-001	IND-STD	IN4454
CR3	GP, 200 mA, 80 V	81-190	IND-STD	IN270
CR4thru CR7	Switching, MF, 10 mA, 75 V	154-3001-001	IND-STD	IN4454
	RELAY			
K1, K2	SPDT, 6V, 325 Ω coil	158-0005-001	29750	2275/6 V

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A3A1	(Cont.)			
	INDUCTORS			
L1 thru L3	Choke Ferrite, RF 750 Ω/50 MHz, ±20%	156-7005-002	02114	VK200-10/3B
L4, L5	7 Turns, #32 Wire Ferrite Core	132-0377-001	03782	132-0377-001
	INTEGRATED CIRCUITS			
MC1	Oper. Amp., 18 V, 250 mW	153-7014-001	27014	LM308H
MC2	DC Amp.	153-7005-001	07263	UA702C/U5B7702393
	TRANSISTORS			
Q1, Q2	15 VC Max, 280 MW, B18-min.	153-3010-001	IND-STD	2N4275
Q3	30 VC Max, 500 MW, B150-300	556-147-059	IND-STD	2N4916
Q4, Q5	15 VC Max, 280 MW, B18-min.	153-3010-001	IND-STD	2N4275
Q6	P Channel, FET, 40 V, 1KμMhos	153-3012-001	IND-STD	2N5460
Q7, Q8	NPN, Silicon, 18 VC Max, 500 MW, B75-min.	153-3003-001	IND-STD	2N5183
Q9	NPN, Silicon, 20 VC Max, 500 MW, B60-1000	153-3009-001	IND-STD	2N5133
Q10	P Channel, FET, 40 V, 1KμMhos	153-3012-001	IND-STD	2N5460
Q11	15 VC Max, 280 MW, B18-min.	153-3010-001	IND-STD	2N4275
Q12	20 VC Max, 200 MW, B25-250	153-3005-001	IND-STD	2N5179
Q13, Q14	15 VC Max, 280 MW, B18-min.	153-3010-001	IND-STD	2N4275
Q15	20 VC Max, 200 MW, B25-250	153-3005-001	IND-STD	2N5179
	RESISTORS			
	NOTE: Unless otherwise specified, all resistors are fixed comp. 1/4 W, ±5%.			
R1	1 KΩ	151-1002-102J	19701	CR25-1-4-5P-1K
R2	18 K	151-1002-183J	19701	CR25-1-4-5P-18K
R3	18 K	151-1002-183J	19701	CR25-1-4-5P-18K
R4	330Ω	151-1002-331J	19701	CR25-1-4-5P-330Ω
R5	1 KΩ	151-1002-102J	19701	CR25-1-4-5P-1K
R6	5600 Ω	151-1002-562J	19701	CR25-1-4-5P-5.6K
R7	1.5 KΩ	151-1002-152J	19701	CR25-1-4-5P-1.5K
R8	5600 Ω	151-1002-562J	19701	CR25-1-4-5P-5.6K

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A3A1	(Cont.)			
R9	6.8 KΩ	151-1002-682J	19701	CR25-1-4-5P-6.8K
R10	1.5 KΩ	151-1002-152J	19701	CR25-1-4-5P-1.5K
R11	22 KΩ	151-1002-223J	19701	CR25-1-4-5P-22K
R12	56 K	151-1002-563J	19701	CR25-1-4-5P-56K
R13	6.2 K	151-1002-622J	19701	CR25-1-4-5P-6.2K
R14	2 K	151-1002-202J	19701	CR25-1-4-5P-2K
R15	1.8 MΩ	151-1002-185J	19701	CR25-1-4-5P-1.8M
R16	10 KΩ	151-1002-103J	19701	CR25-1-4-5P-10K
R17	Factory Selected			
R18	1.8 KΩ	151-1002-182J	19701	CR25-1-4-5P-1.8K
R19	10 KΩ	151-1002-103J	19701	CR25-1-4-5P-10K
R20	1 KΩ	151-1002-102J	19701	CR25-1-4-5P-1K
R21	3.6 K	151-1002-362J	19701	CR25-1-4-5P-3.6K
R22	390 Ω	151-1002-391J	19701	CR25-1-4-5P-390Ω
R23, R24	10 KΩ	151-1002-103J	19701	CR25-1-4-5P-10K
R25	33 KΩ	151-1002-333J	19701	CR25-1-4-5P-33K
R26	10 KΩ	151-1002-103J	19701	CR25-1-4-5P-10K
R27	360 Ω	151-1002-361J	19701	CR25-1-4-5P-360Ω
R28	10 KΩ	151-1002-103J	19701	CR25-1-4-5P-10K
R29	8.2 K	151-1002-822J	19701	CR25-1-4-5P-8.2K
R30, R31	510 Ω	151-1002-511J	19701	CR25-1-4-5P-510Ω
R32	47 Ω	151-1002-473J	19701	CR25-1-4-5P-47K
R33	2 K	151-1002-202J	19701	CR25-1-4-5P-2K
R34	2.7 MΩ	151-1002-275J	19701	CR25-1-4-5P-2.7M
R35	33 KΩ	151-1002-333J	19701	CR25-1-4-5P-33K
R36, R37	1 KΩ	151-1002-102J	19701	CR25-1-4-5P-1K
R38	150 Ω	151-1002-151J	19701	CR25-1-4-5P-150Ω
R39	43 Ω, 1/2 W	151-1003-430J	19701	CR25-1-4-5P-43Ω
R40	680 Ω	151-1002-681J	19701	CR25-1-4-5P-680Ω

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A3A1	(Cont.)			
R41	10 Ω	151-1002-100J	19701	CR25-1-4-5P-10Ω
R42	390 Ω	151-1002-391J	19701	CR25-1-4-5P-390Ω
R43	120 Ω	151-1002-121J	19701	CR25-1-4-5P-120Ω
R44	1 KΩ	151-1002-102J	19701	CR25-1-4-5P-1K
R45	510 Ω	151-1002-511J	19701	CR25-1-4-5P-510Ω
R46 thru R48	1 KΩ	151-1002-102J	19701	CR25-1-4-5P-1K
R49	510 Ω	151-1002-511J	19701	CR25-1-4-5P-510Ω
R50	390 Ω	151-1002-391J	19701	CR25-1-4-5P-390Ω
R51	120 Ω	151-1002-121J	19701	CR25-1-4-5P-120Ω
R52	2.2 K	151-1002-222J	19701	CR25-1-4-5P-2.2K
A3A2	WB P-A MODULATOR	103-1952-002	03782	103-1952-002
	CAPACITORS			
C1, C2	1000 pF, GMV, 500 V, FT, Fixed, Cer.	556-005-381	01121	FA5C/102W
	RESISTORS			
R1	Comp., 39 Ω, ±5%, 1/4W	151-1002-390J	12987	RC07GF390J
R2	Comp., 150 Ω, ±5%, 1/4 W	151-1002-151J	12987	RC07GF151J
A3A2A1	PCA WB PRE-AMP 6201	103-3022-001	03782	103-3022-001
	CAPACITORS			
	NOTE: Unless otherwise specified, all capacitors are fixed ceramic.			
C1 thru C3	0.01 µF, ±20%, 25 V	12-56	71590	UK25-103
C4, C5	.01 µF, ±10%, 200 V	150-1014-103	70371	CM-1712
C6 thru C9	0.01 µF, ±20%, 25 V	12-56	71590	UK25-103
C10	4 pF, ±.25 pF, 500 V	150-1012-40CC	75292	CC20CH040C
C11 thru C13	0.01 µF, ±20%, 25 V	12-56	71590	UK25-103
C14	2 µF, ±.25 pF, 500 V	556-060-166	72982	CC20CK020C

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A3A2A1	(Cont.)			
	INDUCTORS			
L1	7 Turns, #32 Wire, Ferrite Core	132-0377-001	03782	132-0377-001
L2	4 Turns, #22 Wire on 10 MΩ, 1/2 W fixed res.	132-0380-004	03782	132-0380-004
L3	7 Turns, #32 Wire, Ferrite Core	132-0377-001	03782	132-0377-001
L4	1 Turn, #22 Wire on 10 MΩ, 1/2 W fixed res.	132-0380-001	03782	132-0380-001
L5	7 Turns, #32 Wire, Ferrite Core	132-0377-001	03782	132-0377-001
	TRANSISTORS			
Q1, Q2	15 VC, 200 mW, B30-150	153-3032-001	IND-STD	2N2857
	RESISTORS			
	NOTE: Unless otherwise specified, all resistors are fixed 1/4 W, ±1% metal film.			
R1	475 Ω	59-475	19701	MF5C-D-4750F
R2	150 Ω	59-150	19701	RN55-D-1500F
R3	5.62 KΩ	59-562	19701	RN55-D-5621F
R4	1.33 KΩ	59-1.33K	19701	RN55-D-1331F
R5	100 Ω	59-100	19701	MF5C-D-1000F
R6	475 Ω	59-475	19701	MF5C-D-4750F
R7, R8	100 Ω	59-100	19701	MF5C-D-1000F
A3A2A2	BALANCED MODULATOR	103-3107-001	03782	103-3107-001
A3A2A3	BALANCED MODULATOR	103-3107-001	03782	103-3107-001
A3A3	RFI FILTER	103-1953-001	03782	103-1953-001
	CAPACITORS			
C1 thru C3	8500 pF, GMV, 500 V, fixed cer.	150-1013-001	00656	BLF-1CC/852Z
C4 thru C6	1000 pF, GMV, 500 V, fixed cer., FT	556-005-381	01121	FA5C/102W
	INDUCTORS			
L1, L2	7 Turns, #32 Wire, Ferrite Core	132-0377-001	03782	132-0377-001
	RESISTOR			
R1	1 K, ±5%, 1/4 W, Comp.	151-1002-102J	19701	CR25-1-4-5P-1K

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A3A4	FILTER	103-1954-001	03782	103-1954-001
	CAPACITORS			
C1, C2	2500 pF, GMV, 500 V, fixed cer., FT	150-1011-001	00656	BSF-1CC/252Z
C3 thru C6	1000 pF, GMV, 500 V, fixed cer., FT	556-005-381	01121	FA5C/102W
	INDUCTORS			
L1 thru L3	Rf Ferrite Choke, 900 Ω/50MHz, ±20%	156-7005-003	02114	VK200 11/3B
A3A5	FILTER	103-1956-001	03782	103-1956-001
	CAPACITORS			
C1, C2	8500 pF, GMV, 500 V	150-1013-001	00656	BLF-1CC/852Z
	INDUCTORS			
L1, L2	5 Turns, #32 Wire on Closed Ferrite Core	132-0382-002	03782	132-0382-002
A4	POWER AMPLIFIER 6201	103-1955-002	03782	103-1955-002
A4A1	POWER AMPLIFIER 6201	103-3032-001	03782	103-3032-001
	CAPACITORS			
	NOTE: Unless otherwise specified, all capacitors are fixed ceramic.			
C1	.01 µF, ±10%, 150 V	150-1034-001	72982	8141-M100-C0G-103K
C2	.01 µF, ±0%, 200 V	150-1014-103	70371	CM1712
C3	.01 µF, ±10%, 150 V	150-1034-001	72982	8141-M100-C0G-103K
C4, C5	.01 µF, ±0%, 200 V	150-1014-103	70371	CM1712
C6	.01 µF, ±10%, 150 V	150-1034-001	72982	8141-M100-C0G-103K
C7	.001 µF, ±0%, 1000 V	556-060-046	71590	DD102
C8	.01 µF, ±10%, 150 V	150-1034-001	72982	8141-M100-C0G-103K
C9	4 pF, ±.25 pF, 500 V	150-1012-40CC	75292	CC20CH040C
C10	.001µF, ±0%, 1000 V	556-060-046	71590	DD102
C11	.01 µF, ±0%, 200 V	150-1014-103	70371	CM1712
C12	.022 µF, ±20%, 25 V	556-060-105	71590	UK25-223
C13	.01 µF, ±10%, 150 V	150-1034-001	72982	8141-M100-C0G-103K
C14	27 pF, ±2%, 500 V	150-2002-270EG0	14655	CD15ED270G03
C15	12 pF, ±5%, 500 V DM	150-2002-120CJ0	14655	CD15CD120J03

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A4A1	(Cont.)			
C16	4 pF, ±.25 pF, 500 V	150-1012-40CC	75292	CC20CH040C
C17	.01 µF, ±10%, 150 V	150-1034-001	72982	8141-M100-C0G-103K
C18	.01 µF, ±10%, 200 V	150-1014-103	70371	CM1712
C19	.022 µF, ±20%, 25 V	556-060-105	71590	UK25-223
C20	.001 µF, ±10%, 1000 V	556-060-046	71590	DD102
C21	.022 µF, ±20%, 25 V	556-060-105	71590	UK25-223
C22, C23	.01 µF, ±10%, 150 V	150-1034-001	72982	8141-M100-C0G-103K
C24	6 pF, ±.25%, 500 V	150-1012-060CC	75292	CC20CH060C
C25, C26	12 pF, ±5%, 500 V DM	150-2002-120CJ0	14655	CD15CD120J03
C27	.022 µF, ±20%, 25 V	556-060-105	71590	UK25-223
C28	.001 µF, ±10%, 1000 V	556-060-046	71590	DD102
C29	100 pF, ±2%, 500 V DM	150-2002-220EG0	72136	DM15E220G0
C30	.01 µF, ±10%, 200 V	150-1014-103	70371	CM1712
C31	.001 µF, ±10%, 1000 V	556-060-046	71590	DD102
C32, C33	.01 µF, ±10%, 150 V	150-1034-001	72982	8141-M100-C0G-103K
C34	100 pF, ±2%, 500 V DM	150-2002-220EG0	72136	DM15E220G0
C35	4 pF, ±.25 pF, 500 V	150-1012-40CC	75292	CC20CH040C
C36	.022 µF, ±20%, 25 V	556-060-105	71590	UK25-223
C37	.001 µF, ±10%, 1000 V	556-060-046	71590	DD102
C38	.01 µF, ±10%, 200 V	150-1014-103	70371	CM1712
C39	.01 µF, ±10%, 150 V	150-1034-001	72982	8141-M100-C0G-103K
C40	.001 µF, ±10%, 1000 V	556-060-046	71590	DD102
C41	.022 µF, ±20%, 25 V	556-060-105	71590	UK25-223
C42	.01 µF, ±10%, 150 V	150-1034-001	72982	8141-M100-C0G-103K
C43	47 pF, ±2%, 500 V	150-2002-470EG0	14655	CD15ED470G03
C44	39 pF, ±2%, 500 V	150-2002-390EG0	72136	CD15ED390G03
C45	5 pF, ±.25 pF, 500 V	556-060-109	75292	CC20CH050C
C46	4 pF, ±.25 pF, 500 V	150-1012-40CC	75292	CC20CH040C
C47	.1 µF, ±20%, 25 V	556-120-162	56289	5C023104X0250B3

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A4A1	(Cont.)			
C48	.001 μF, ±10%, 1000 V	556-060-046	71590	DD102
C49	.022 μF, ±20%, 25 V	556-060-105	71590	UK25-223
C50	.01 μF, ±10%, 200 V	150-1014-103	70371	CM1712
C51	.001 μF, ±10%, 1000 V	556-060-046	71590	DD102
C52	.01 μF, ±10%, 150 V	150-1034-001	72982	8141-M100-C0G-103K
C53	.01 μF, ±10%, 200 V	150-1014-103	70371	CM1712
C54	6 pF, ±.25%, 500 V	150-1012-060CC	75292	CC20CH060C
C55	36 pF, ±2%, 500 V	150-2002-360EJ0	14655	CD15ED360G03
C56	6 pF, ±.25 pF, 500 V	150-1012-060CC	75292	CC20CH060C
C57	.001 μF, ±10%, 1000 V	556-060-046	71590	DD102
C58	.022 μF, ±20%, 25 V	556-060-105	71590	UK25-223
C59	.01 μF, ±10%, 150 V	150-1034-001	72982	8141-M100-C0G-103K
C60	1 μF, ±20%, 50 V	12-94	72982	8131-M050-651-105M
C61, C62	.01 μF, ±10%, 200 V	150-1014-103	70371	CM1712
C63	.001 μF, ±10%, 1000 V	556-060-046	71590	DD102
C64	1 μF, ±20%, 50 V	12-94	72982	8131-M050-651-105M
C65	.001 μF, ±10%, 1000 V	556-060-046	71590	DD102
C66	.022 μF, ±20%, 25 V	556-060-105	71590	UK25-223
C67, C68	.01 μF, ±10%, 150 V	150-1034-001	72982	8141-M100-C0G-103K
C69	.001 μF, ±10%, 1000V	556-060-046	71590	DD102
C70	2 μF, ±.25 pF, 500 V	556-060-166	72982	CC20CK020C
C71 thru C74	1000 pF, GMV, 500 V, FT	556-005-381	01121	FA5C/102W
C75	.001 μF, ±10%, 1000 V	556-060-046	71590	DD102
	DIODE			
CR1	Switching, MF, 10 mA, 75 V	154-3001-001	IND-STD	IN4454
	CONNECTOR			
J1	Receptacle, Coax. 50 Ω	556-205-001	98291	51-051-000
	INDUCTORS			
L1	4 Turns, #22 Wire on 10 MΩ, 1/2 W fixed res.	132-0380-004	03782	132-0380-004
L2	7 Turns, #32 Wire, Ferrite Core	132-0377-001	03782	132-0377-001
L3	4 Turns, #22 Wire on 10 MΩ, 1/2 W fixed res.	132-0380-004	03782	132-0380-004

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A4A1	(Cont.)			
L4	7 Turns, #32 Wire, Ferrite Core	132-0377-001	03782	132-0377-001
L5	1 Turn, #22 Wire on 10 MΩ, 1/2 W fixed res.	132-0380-001	03782	132-0380-001
L6 , L7	3 Turns, #22 Wire on 10 MΩ, 1/2 W comp res.	132-0380-003	03782	132-0380-003
L8	7 Turns, #32 Wire, Ferrite Core	132-0377-001	03782	132-0377-001
L9	2 Turns, #22 Wire on 10 MΩ, 1/2 W fixed res.	132-0380-002	03782	132-0380-002
L10	7 Turns, #32 Wire, Ferrite Core	132-0377-001	03782	132-0377-001
L11	4 Turns, #22 Wire on 10 MΩ, 1/2 W fixed res.	132-0380-004	03782	132-0380-004
L12	3 Turns, #22 Wire on 10 MΩ, 1/2 W comp res.	132-0380-003	03782	132-0380-003
L13	RF 750 Ω/50MZ, ±20%, Choke Ferrite	156-7005-002	02114	VK200-10/3B
L14	1 Turn, #22 Wire on 10 MΩ, 1/2 W fixed res.	132-0380-001	03782	132-0380-001
L15, L16	RF 750 Ω/50 MHz, ±20%, Choke Ferrite	156-7005-002	02114	VK200-10/3B
L17	4 Turns, #22 Wire on 10 MΩ, 1/2 W fixed res.	132-0380-004	03782	132-0380-004
L18	RF 750 Ω/50 MHz, ±20%, Choke Ferrite	156-7005-002	02114	VK200-10/3B
L19	7 Turns, #32 Wire, Ferrite Core	132-0377-001	03782	132-0377-001
L20	1 Turn, #22 Wire on 10 MΩ, 1/2 W fixed res.	132-0380-001	03782	132-0380-001
L21	RF 750 Ω/50 MHz, ±20%, Choke Ferrite	156-7005-002	02114	VK200-10/3B
L22	2 Turns, #22 Wire on 10 MΩ, 1/2 W fixed res.	132-0380-002	03782	132-0380-002
L23	3 Turns, #22 Wire on 10 MΩ, 1/2 W comp res.	132-0380-003	03782	132-0380-003
L24	4 Turns, #22 Wire on 10 MΩ, 1/2 W fixed res.	132-0380-004	03782	132-0380-004
L25, L26	RF 750 Ω/50 MHz, ±20%, Choke Ferrite	156-7005-002	02114	VK200-10/3B
L27	7 Turns, #32 Wire, Ferrite Core	132-0377-001	03782	132-0377-001
L28	1 Turn, #22 Wire on 10 MΩ, 1/2 W fixed res.	132-0380-001	03782	132-0380-001
L29	RF 750 Ω/50 MHz, ±20%, Choke Ferrite	156-7005-002	02114	VK200-10/3B
L30	3 Turns, #22 Wire on 10 MΩ, 1/2 W comp res.	132-0380-003	03782	132-0380-003
L31	RF 750 Ω/50 MHz, ±20%, Choke Ferrite	156-7005-002	02114	VK200-10/3B
L32, L33	7 Turns, #32 Wire, Ferrite Core	132-0377-001	03782	132-0377-001
L34	RF 750 Ω/50 MHz, ±20%, Choke Ferrite	156-7005-002	02114	VK200-10/3B
L35	7 Turns, #32 Wire, Ferrite Core	132-0377-001	03782	132-0377-001
L36	2 Turns, #22 Wire on 10 MΩ, 1/2 W fixed res.	132-0380-002	03782	132-0380-002

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A4A1	(Cont.)			
L37	RF 750 Ω/50 MHz, ±20%, Choke Ferrite	156-7005-002	02114	VK200-10/3B
L38	7 Turns, #32 Wire, Ferrite Core	132-0377-001	03782	132-0377-001
L39	Shielded, 27 μH/1.15 Ω, ±5%, 530 mA	156-7002-030	36196	DINK-27
L40	RF 750 Ω/50 MHz, ±20%, Choke Ferrite	156-7005-002	02114	VK200-10/3B
	TRANSISTORS			
Q1 thru Q4	15 VC, 200 MW, B30-150	153-3032-001	IND-STD	2N2857
Q5	20 VC, 3.5 W, B10-200	153-3030-001	IND-STD	2N4427
Q6	20 VC, 3.5 W, B70-210	81-271	IND-STD	2N5109
Q7	Pwr, NPN, Silicon, 12 W	153-5010-001	93702	D5E
	RESISTORS			
	NOTE: Unless otherwise specified, all resistors are fixed comp. 1/4 W, ±5 %.			
R1	150 Ω, ±1% MF	59-150	19701	RN55-D-1500F
R2	475 Ω, ±1% MF	59-475	19701	MF5C-D-4750F
R3	1.02 KΩ, ±1%, 1/4 W	59-1.02K	19701	RN55-D-1021F
R4	105 Ω, ±1%, MF	59-105	19701	RN55-D-1050F
R5	560 Ω	151-1002-561J	19701	CR25-1-4-5P-560Ω
R6	68 Ω	151-1002-680J	19701	CR25-1-4-5P-68Ω
R7	105 Ω, ±1% MF	59-105	19701	RN55-D-1050F
R8	475 Ω, ±1%, MF	59-475	19701	MF5C-D-4750F
R9	51 Ω	151-1002-510J	19701	CR25-1-4-5P-51Ω
R10	56 Ω	151-1002-560J	19701	CR25-1-4-5P-56Ω
R11	820 Ω	151-1002-821J	19701	CR25-1-4-5P-820Ω
R12	430Ω	151-1002-431J	19701	CR25-1-4-5P-430Ω
R13	22 Ω	151-1002-220J	19701	CR25-1-4-5P-22Ω
R14	165 Ω, ±1% MF	59-165	19701	RN55-D-1650F
R15	249 Ω, ±1% MF	59-249	19701	RN55-D-2490F
R16	90.9 Ω, ±1%, MF	59-90.9	19701	RN55-D-90R9F
R17	56 Ω	151-1002-560J	19701	CR25-1-4-5P-56Ω

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A4A1	(Cont.)			
R18	18 Ω	151-1002-180J	19701	CR25-1-4-5P-18Ω
R19	820 Ω	151-1002-821J	19701	CR25-1-4-5P-820Ω
R20	430 Ω	151-1002-431J	19701	CR25-1-4-5P-430Ω
R21, R22	75 Ω	151-1002-750J	19701	CR25-1-4-5P-75Ω
R23	324 Ω, ±1% MF	59-324	19701	RN55-D-3240F
R24	21.5 Ω, ±1% MF	59-21.5	19701	RN55-D-21R5F
R25	680 Ω	151-1002-681	19701	CR25-1-4-5P-680Ω
R26	309 Ω, ±1% MF	59-309	19701	RN55-D-3090F
R27	48.7 Ω, ±1% MF	59-48.7	19701	RN55-D-48R7F
R28	100 Ω	151-1003-101J	19701	CR25-1-4-5P-100Ω
R29	56 Ω	151-1002-560J	19701	CR25-1-4-5P-56Ω
R30	68 Ω	151-1002-680 Ω	19701	CR-1-4-5P-68Ω
R31	820 Ω	151-1002-821J	19701	CR25-1-4-5P-820Ω
R32	61.9 Ω, ±1% MF	59-61.9	19701	RN55-D-61R9F
R33	48.7 Ω, ±1% MF	59-48.7	19701	RN55-D-48R7F
R34	39 Ω	151-1002-390J	12987	RC07GF390J
R35	33 Ω	151-1002-330J	19701	CR25-1-4-5P-33Ω
R36	56 Ω	151-1002-560J	19701	CR25-1-4-5P-56Ω
R37	510 Ω	151-1002-511J	19701	CR25-1-4-5P-510Ω
R38	24.9 Ω, ±1% MF	59-24.9	19701	RN55-D-24R9F
R39	39 Ω	151-1002-390J	12987	RC07GF390J
R40	22Ω, 1W	151-1004-220J	MILPN	RC32GF220J
R41	1.5 KΩ	151-1002-152J	19701	CR25-1-4-5P-1.5K
R42	56 Ω	151-1002-560J	19701	CR25-1-4-5P-56Ω
A5	LOW PASS FILTER	103-2161-001	03782	103-2161-001
A5A1	FEED PLATE ASSEMBLY	103-1925-001	03782	103-1925-001
	RELAYS			
K1 thru K5	Switch, RF Low Level, .01 A at 28 V, Cont. 35 at pull in	161-5001-001	12617	MTRF2/37.5 at Max

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A5A1A1	LO PASS FILTER	103-1829-001	03782	103-1829-001
	CAPACITORS			
C1	.01 μF, ±10%, 200 V, fixed cer.	150-1014-103	70371	CM1712
C2	2 μF, ± .25 pF, 500 V, fixed cer.	556-060-166	72982	CC20CK020C
	RELAY			
K6	SPST Min Reed 0.5 A at 200 V	161-5002-001	12617	MRR-2/35 at Max
	RESISTORS			
R1	68 Ω, ±5%, 1/4 W, Comp.	151-1002-680J	19701	CR25-1-4-5P-68Ω
R2, R3	51.1 Ω, ±1%, 1/2 W, MF	151-2018-51R1	28363	C5/51.1/1%
A5A1A1A1	DETECTOR, PEAK	103-1897-001	03782	103-1897-001
	CAPACITOR			
C1	470 pF, ±10%, 300 V, Cer. FT	150-1009-001	01121	FW5N-4712/M-6447
	DIODE			
CR1	Hot Carr, 70 V, 250 mW	154-4001-001	28480	5082-2800
	RESISTOR			
R1	100 Ω, ±5%, 1/8 W, Comp.	151-1016-101J	19701	CR16-1-8-5P-100Ω
A5A1A2	RELAY DRIVER	103-1830-001	03782	103-1830-001
	DIODES			
CR1 thru CR3	Switching, MF, 10 mA, 75 V	154-3001-001	IND-STD	1N4454
	TRANSISTORS			
Q1	NPN, Silicon, 20 VC Max, 500 mW, B60-1000	153-3009-001	IND-STD	2N5133
Q2, Q3	NPN, Silicon, 18 VC Max, 500 mW, B75-min.	153-3003-001	IND-STD	2N5183
	RESISTORS			
R1	1 KΩ, ±5%, 1/4 W, Fixed Comp.	151-1002-102J	19701	CR25-1-4-5P-1K
R2	10 KΩ, ±5%, 1/4 W, Fixed Comp.	151-1002-103J	19701	CR25-1-4-5P-10K
R3	1.5 KΩ, ±5%, 1/4 W, Fixed Comp.	151-1002-152J	19701	CR25-1-4-5P-1.5K
A5A1A3	LO PASS FILTER	103-1828-001	03782	103-1828-001
A5A2	BAND SWITCH	103-2150-001	03782	103-2150-001
A5A2A1	COVER & FILTER	103-2095-001	03782	103-2095-001

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A5A3	BAND SWITCH	103-2149-001	03782	103-2149-001
	DIODES			
CR1	Switching, MF, 10 mA, 75 V	154-3001-001	IND-STD	IN4454
CR2	G.P., 600 V, 1 A	81-20	IND-STD	IN4005
CR3 thru CR15	Switching, MF, 10 mA, 75 V	154-3001-001	IND-STD	IN4454
	INTEGRATED CIRCUITS			
IC1	Quad 2-Input Nand Gates	153-7031-001	01295	SN5400N
IC2	Hex Inverter, DTμ L9935N	153-7042-001	07263	U6A993559
	RESISTORS			
R1 thru R6	5600 Ω, ±5%, 1/4 W, Comp.	151-1002-562J	19701	CR25-1-4-5P-5.6K
R7	200 Ω, ±5%, 1/4 W, Comp.	151-1002-201J	19701	CR25-1-4-5P-200Ω
R8 thru R14	5600 Ω, ±5%, 1/4 W, Comp	151-1002-562J	19701	CR25-1-4-5P-5.6K
	SOCKET			
XIC1,2	DIP 14 Contact	167-0009-002	23880	CSA2900-14B

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A5A4	ROTOR ASSEMBLY	103-1921-001	03782	103-1921-001
	CAPACITORS			
	NOTE: Unless otherwise specified, all capacitors are fixed DM.			
C1	NOT ASSIGNED			
C2	NOT ASSIGNED			
C3	5 pF, ±.25 pF, 500 V, fixed cer.	556-060-109	75292	CC20CH050C
C4	15 pF, ±5%, 500 V	150-2002-150CJ0	72136	DM15C150J0500
C5	20 pF, ±2%, 500 V	150-2002-200EG0	72136	CD15CD200G03
C6	30 pF, ±2%, 500 V	150-2002-300EG0	72136	DM15E300G0500
C7	43 pF, ±2%, 500 V	150-2002-430EG0	72136	DM15E430G0
C8	56 pF, ±2%, 500 V	150-2002-560EG0	72136	DM15E560G0500
C9	82 pF, ±2%, 500 V	150-2002-820EG0	72136	CD153D820G03
C10	160 pF, ±2%, 500 V	150-2002-161FG0	72136	DM15F161G0500
C11	300 pF, ±2%, 500 V	150-2002-301FG0	14655	CD15FD301G03
C12	30 pF, ±2%, 500 V	150-2002-300EG0	72136	DM15E300G0500
A5A4A1	LO PASS FILTER 1	103-1908-001	03782	103-1908-001
	CAPACITORS			
C1	NOT ASSIGNED			
C2	NOT ASSIGNED			
C3	9 pF, ±.25 pF, 500 V, fixed cer.	150-1012-090CC	75292	CC20CH090C
C4	NOT ASSIGNED			
C5	9 pF, ±.25 pF, 500 V, fixed cer.	150-1012-090CC	75292	CC20CH090C
C6	NOT ASSIGNED			
C7	9 pF, ±.25 pF, 500 V, fixed cer.	150-1012-090CC	75292	CC20CH090C
	INDUCTORS			
L1	NOT ASSIGNED			
L2	NOT ASSIGNED			
L3	NOT ASSIGNED			
L4	4 Turns, #24 Wire on .156" Dia. X 1/2" Long	132-0371-003	03782	132-0371-003
L5	NOT ASSIGNED			

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A5A4A1	(Cont.)			
L6	4 Turns, #24 Wire on .156" dia. X 1/2" Long	132-0371-003	03782	132-0371-003
A5A4A2	LO PASS FILTER 1	103-1907-001	03782	103-1907-003
	CAPACITORS			
C1	NOT ASSIGNED			
C2	NOT ASSIGNED			
C3	3 pF, ± .25 pF, 500 V, fixed cer.	556-060-127	75292	CC20CJ030C
C4	NOT ASSIGNED			
C5	3 pF, ± .25 pF, 500 V, fixed cer.	556-060-127	75292	CC20CJ030C
C6	NOT ASSIGNED			
C7	2 pF, ± .25 pF, 500 V, fixed cer.	556-060-166	72982	CC20CK020C
	INDUCTORS			
L1	NOT ASSIGNED			
L2	NOT ASSIGNED			
L3	NOT ASSIGNED			
L4	5 Turns, #20 Wire on .156" Dia. X 1/2" Long	132-0371-002	03782	132-0371-002
L5	NOT ASSIGNED			
L6	5 Turns, #20 Wire on .156" Dia. X 1/2" Long	132-0371-002	03782	132-0371-002
A5A4A3	LO PASS FILTER 2	103-1910-001	03782	103-1910-001
	CAPACITORS			
C1	NOT ASSIGNED			
C2	NOT ASSIGNED			
C3	12 pF, ±5%, 500 V, fixed DM	150-2002-120CJ0	14655	CD15CD120J03
C4	NOT ASSIGNED			
C5	15 pF, ±5%, 500 V, fixed DM	150-2002-150CJ0	72136	DM15C150J0500
C6	NOT ASSIGNED			
C7	15 pF, ±5%, 500 V, fixed DM	150-2002-150CJ0	72136	DM15C150J0500
	INDUCTORS			
L1	NOT ASSIGNED			
L2	8 Turns, #24 Wire on .156" Dia. X 1/2" Long	132-0371-016	03782	132-0371-016

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A5A4A3	(Cont.)			
L3	NOT ASSIGNED			
L4	9 Turns, #24 Wire on .156" Dia. X 1/2" Long	132-0371-011	03782	132-0371-011
L5	NOT ASSIGNED			
L6	9 Turns, #24 Wire on .156" Dia. X 1/2" Long	132-0371-011	03782	132-0371-011
L7	NOT ASSIGNED			
L8	7 Turns, #24 Wire on .156" Dia. X 1/2" Long	132-0371-012	03782	132-0371-012
A5A4A4	LO PASS FILTER 2	103-1909-001	03782	103-1909-001
	CAPACITORS			
C1	NOT ASSIGNED			
C2	NOT ASSIGNED			
C3	10 pF, ± .25 pF, 500 V, fixed cer.	150-1012-100CC	75292	CC20CH100C
C4	NOT ASSIGNED			
C5	10 pF, ±1/2 pF, 500 V, fixed DM	150-2002-100CG0	14655	CD15CD100D03
C6	NOT ASSIGNED			
C7	8 pF, ± .25 pF, 500 V, fixed cer.	150-1012-080CC	75292	CC20CH080C
	INDUCTORS			
L1	NOT ASSIGNED			
L2	5 Turns, #24 Wire on .156" Dia. X 1/2" Long	132-0371-007	03782	132-0371-007
L3	NOT ASSIGNED			
L4	6 Turns, #24 Wire on .156" Dia. X 1/2" Long	132-0371-009	03782	132-0371-009
L5	NOT ASSIGNED			
L6	6 Turns, #24 Wire on .156" Dia. X 1/2" Long	132-0371-009	03782	132-0371-009
L7	NOT ASSIGNED			
L8	4 1/2 Turns, #24 Wire on .156" Dia. X 1/2" Long	132-0371-004	03782	132-0371-004
A5A4A5	LO PASS FILTER 3	103-1912-001	03782	103-1912-001
	CAPACITORS			
C1	NOT ASSIGNED			
C2	NOT ASSIGNED			
C3	33 pK, ±2%, 500 V, fixed DM	150-2002-330EG0	14655	CD15ED330G03

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A5A4A5	(Cont.)			
C4	NOT ASSIGNED			
C5	30 pF, ±2%, 500 V, fixed DM	150-2002-300EG0	72136	DM15E300G0500
C6	NOT ASSIGNED			
C7	27 pF, ±2%, 500 V, fixed DM	150-2002-270EG0	14655	CD15ED270G03
	INDUCTORS			
L1	NOT ASSIGNED			
L2	11 Turns, #27 Wire on .156" Dia. X 1/2" Long	132-0371-018	03782	132-0371-018
L3	NOT ASSIGNED			
L4	13 Turns, #27 Wire on .156" Dia. X 1/2" Long	132-0371-021	03782	132-0371-021
L5	NOT ASSIGNED			
L6	13 1/2 Turns, #27 Wire on .156" Dia. X 1/2" Long	132-0371-023	03782	132-0371-023
L7	NOT ASSIGNED			
L8	9 Turns, #27 Wire on .156" Dia. X 1/2" Long	132-0371-014	03782	132-0371-014
A5A4A6	LO PASS FILTER 3	103-1911-001	03782	103-1911-001
	CAPACITORS			
C1	NOT ASSIGNED			
C2	NOT ASSIGNED			
C3	24 pF, ±5%, 500 V, fixed DM	150-2002-240EG0	72136	CD15ED240J03
C4	NOT ASSIGNED			
C5	100 pF, ±2%, 500 V, fixed DM	150-2002-220EG0	72136	DM15E220G0
C6	NOT ASSIGNED			
C7	18 pF, ±2%, 500 V, fixed DM	150-2002-180CG0	14655	CM05CD180G03
	INDUCTORS			
L1	NOT ASSIGNED			
L2	11 Turns, #24 Wire on .156" Dia. X 1/2" Long	132-0371-013	03782	132-0371-013
L3	NOT ASSIGNED			
L4	10 Turns, #27 Wire on .156" Dia X 1/2" Long	132-0371-015	03782	132-0371-015
L5	NOT ASSIGNED			
L6	10 Turns, #27 Wire on .156" Dia. X 1/2" Long	132-0371-015	03782	132-0371-015

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A5A4A6	(Cont.)			
L7	NOT ASSIGNED			
L8	9 Turns, #24 Wire on .156" Dia. X 1/2" Long	132-0371-011	03782	132-0371-011
A5A4A7	LO PASS FILTER 4	103-1914-001	03782	103-1914-001
	CAPACITORS			
C1	NOT ASSIGNED			
C2	NOT ASSIGNED			
C3	68 pF, ±2%, 500 V, fixed DM	150-2002-680EG0	14655	CD15ED680G03
C4	NOT ASSIGNED			
C5	62 pF, ±2%, 500 V, fixed DM	150-2002-620EG0	14655	CD15ED620G03
C6	NOT ASSIGNED			
C7	51 pF, ±2%, 500 V, fixed DM, Elec.	150-2002-510EG0	14655	CD15ED510G03
	INDUCTORS			
L1	NOT ASSIGNED			
L2	18 Turns, #27 Wire on .156" Dia. X 1/2" Long	132-0371-029	03782	132-0371-029
L3	NOT ASSIGNED			
L4	20 Turns, #30 Wire on .156" Dia. X 1/2" Long	132-0371-030	03782	132-0371-030
L5	NOT ASSIGNED			
L6	20 Turns, #30 wire on .156" Dia. X 1/2" Long	132-0371-030	03782	132-0371-030
L7	NOT ASSIGNED			
L8	16 Turns, #27 Wire on .156" Dia. X 1/2" Long	132-0371-026	03782	132-0371-026
A5A4A8	LO PASS FILTER 4	103-1913-001	03782	103-1913-001
	CAPACITORS			
C1	NOT ASSIGNED			
C2	NOT ASSIGNED			
C3	47 pF, ±2%, 500 V, fixed DM	150-2002-470EG0	14655	CD15ED470G03
C4	NOT ASSIGNED			
C5	43 pF, ±2%, 500 V, fixed DM	150-2002-430EG0	72136	DM15E430G0
C6	NOT ASSIGNED			
C7	36 pF, ±2%, 500 V, fixed DM	150-2002-360EJ0	14655	CD15ED360G03

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A5A4A8	(Cont.)			
	INDUCTORS			
L1	NOT ASSIGNED			
L2	15 Turns, #27 Wire on .156" Dia. X 1/2" Long	132-0371-024	03782	132-0371-024
L3	NOT ASSIGNED			
L4	17 Turns, #27 Wire on .156" Dia. X 1/2" Long	132-0371-027	03782	132-0371-027
L5	NOT ASSIGNED			
L6	17 Turns , #27 Wire on .156" Dia. X 1/2" Long	132-0371-027	03782	132-0371-027
L7	NOT ASSIGNED			
L8	13 Turns, #27 Wire on .156" Dia. X 1/2" Long	132-0371-021	03782	132-0371-021
A5A4A9	LO PASS FILTER 5	103-1916-001	03782	103-1916-001
	CAPACITORS			
C1	NOT ASSIGNED			
C2	NOT ASSIGNED			
C3	130 pF, ±2%, 500 V, fixed DM	150-2002-131FG0	72136	DM15F131G0500
C4	NOT ASSIGNED			
C5	130 pF, ±2%, 500 V, fixed DM	150-2002-131FG0	72136	DM15F131G0500
C6	NOT ASSIGNED			
C7	100 pF, ±2%, 500 V, fixed DM	150-2002-101FG0	14655	CD15FD101G03
	INDUCTORS			
L1	NOT ASSIGNED			
L2	26 Turns, #30 Wire on .156" Dia. X 1/2" Long	132-0371-037	03782	132-0371-037
L3	NOT ASSIGNED			
L4	29 Turns, #34 Wire on .156" Dia. X 1/2" Long	132-0371-039	03782	132-0371-039
L5	NOT ASSIGNED			
L6	30 Turns, #34 Wire on .156" Dia. X 1/2" Long	132-0371-042	03782	132-0371-042
L7	NOT ASSIGNED			
L8	22 Turns, #30 Wire on .156" Dia. X 1/2" Long	132-0371-033	03782	132-0371-033
A5A4A10	LO PASS FILTER 5	103-1915-001	03782	103-1915-001

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A5A4A10	(Cont.)			
	CAPACITORS			
C1	NOT ASSIGNED			
C2	NOT ASSIGNED			
C3	91 pF, ±2%, 500 V, fixed DM	150-2002-910FG0	72136	DM15F910G0500
C4	NOT ASSIGNED			
C5	91 pF, ±2%, 500 V, fixed DM	150-2002-910FG0	72136	DM15F910G0500
C6	NOT ASSIGNED			
C7	75 pF, ±2%, 500 V, fixed DM	150-2002-750EG0	72136	CD15ED750G03
	INDUCTORS			
L1	NOT ASSIGNED			
L2	21 Turns, #30 Wire on .56" Dia. X 1/2" Long	132-0371-032	03782	132-0371-032
L3	NOT ASSIGNED			
L4	22 Turns, #30 Wire on .156" Dia. X 1/2" Long	132-0371-033	03782	132-0371-033
L5	NOT ASSIGNED			
L6	24 Turns, #30 Wire on .156" Dia. X 1/2" Long	132-0371-036	03782	132-0371-036
L7	NOT ASSIGNED			
L8	15 Turns, #30 Wire on .156" Dia. X 1/2" Long	132-0371-025	03782	132-0371-025
A5A4A11	LO PASS FILTER 6	103-1918-001	03782	103-1918-001
	CAPACITORS			
C1	NOT ASSIGNED			
C2	NOT ASSIGNED			
C3	270 pF, ±2%, 500 V, fixed DM	150-2002-271FG0	72136	D15F271G0500
C4	NOT ASSIGNED			
C5	240 pF, ±2%, 500 V, fixed DM	150-2002-241FG0	72136	DM15F271G0500
C6	NOT ASSIGNED			
C7	20 pF, ±2%, 500V, fixed DM	150-2002-201FG0	14655	CM05FD201G03
	INDUCTORS			
L1	NOT ASSIGNED			
L2	33 Turns, #34 Wire on .156" Dia. X 1/2" Long	132-0371-043	03782	132-0371-043

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A5A4A11	(Cont.)			
L3	NOT ASSIGNED			
L4	39 Turns, #34 Wire on .156" Dia. X 1/2" Long	132-0371-045	03782	132-0371-045
L5	NOT ASSIGNED			
L6	40 Turns, #34 Wire on .156" Dia. X 1/2" Long	132-0371-046	03782	132-0371-046
L7	NOT ASSIGNED			
L8	29 Turns, #34 Wire on .156" Dia. X 1/2" Long	132-0371-040	03782	132-0371-040
A5A4A12	LO PASS FILTER 6	103-1917-001	03782	103-1917-001
	CAPACITORS			
C1	NOT ASSIGNED			
C2	NOT ASSIGNED			
C3	180 pF, ±2%, 500 V, fixed DM	150-2002-181FG0	72136	CD15FD181G03
C4	NOT ASSIGNED			
C5	180 pF, ±2%, 500 V, fixed DM	150-2002-181FG0	72136	CD15FD181G03
C6	NOT ASSIGNED			
C7	150 pF, ±2%, 500 V, fixed DM	150-2002-151FG0	72136	DM15F151G0500
	INDUCTORS			
L1	NOT ASSIGNED			
L2	27 Turns, #34 Wire on .156" Dia. X 1/2" Long	132-0371-038	03782	132-0371-038
L3	NOT ASSIGNED			
L4	30 Turns, #34 Wire on .156" Dia. X 1/2" Long	132-0371-041	03782	132-0371-041
L5	NOT ASSIGNED			
L6	33 Turns, #34 Wire on .156" Dia. X 1/2" Long	132-0371-043	03782	132-0371-043
L7	NOT ASSIGNED			
L8	23 Turns, #34 Wire on .156" Dia. X 1/2" Long	132-0371-035	03782	132-0371-035
A5A5	BAND SWITCH	103-3067-001	03782	103-3067-001
	CAPACITORS			
C1, C2	33 µF, ±20%, 25 V, fixed cer.	13-91	56289	196D336X0025LA3
	TRANSISTOR			
Q1	0.31 W, 40 VC Max. B100-300	556-146-989	IND-STD	2N3904

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A5A5	(Cont.)			
	RESISTORS			
	NOTE: Unless otherwise specified, all resistors are fixed 1/4 W, ±1% metal film.			
R1	3.40 KΩ	59-3.40K	19701	MF5C-D-3401F
R2	14.0 KΩ	59-14.0K	19701	RN55-D-1402F
R3	2 KΩ	59-2.00K	19701	MF5C-D-2001F
R4	28 KΩ	59-28.0K	19701	RN55-D-2802F
R5	30.1 KΩ	59-30.1K	19701	RN55-D-3012F
R6	59.0 KΩ	59-59.0K	19701	RN55-D-5902F
R7	75.0 KΩ	59-75.0K	19701	RN55-D-7502F
R8	51.1 KΩ	59-51.1K	19701	MF5C-D-5112F
R9, R10	127 K	59-127K	19701	RN55-D-1273F
R11	2.61 KΩ	59-2.61K	19701	RN55-D-2611F
R12	NOT ASSIGNED			
R13	26.7 KΩ	59-26.7K	19701	RN55-D-2672F
	SWITCH			
S1	Switch Wafer	133-0108-001	03782	133-0108-001
A6	ATTENUATOR ASSEMBLY			
A6A1	ATTENUATOR 80 dB	103-2101-002	03782	103-2101-002
A6A1A1	COVER/FILTER 80 dB ATTENUATOR	103-2100-002	03782	103-2100-002
A6A1A1A1	PHOTOXSTOR	103-2097-002	03782	103-2097-002
	TRANSISTORS			
Q1	Photo NPN	153-8001-001	07263	FPT100
Q2, Q3	NPN, Silicon, 20 VC Max, 500 mW, B60-1000	153-3009-001	IND-STD	2N5133
Q4 thru Q7	Difused Silicon, 30 VC Max, 500 mW, B150-300	556-147-059	IND-STD	2N4916
	RESISTORS			
R1	22 KΩ, ±5%, 1/4 W, Comp.	151-1002-223J	19701	CR25-1-4-5P-22K
R2, R3	1.8 KΩ, ±5%, 1/4 W, Comp.	151-1002-182J	19701	CR25-1-4-5P-1.8K

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A6A1A1A1	(Cont.)			
R4, R5	1.5 KΩ, ±5%, 1/4 W, Comp.	151-1002-152J	19701	CR25-1-4-5P-1.5K
R6, R7	47 KΩ, ±5%, 1/4 W, Comp.	151-1002-473J	19701	CR25-1-4-5P-47K
A6A1A1A2	LAMP	103-2102-001	03782	103-2102-001
	INDICATOR			
DS1	Lamp, .04A, 6.3 V	160-6007-001	71744	2180
	RESISTOR			
R1	22 Ω , ±5%, 1/4 W, Comp.	151-1002-220J	19701	CR25-1-4-5P-22Ω
A6A1A1A3	CASE, FILTER	103-1934-001	03782	103-1934-001
	CAPACITOR			
C8	8500 pF, GMV, 500 V, fixed cer.	150-1013-001	00656	BLF-1CC/852Z
A6A1A2	MOUNTING PLATE	103-2103-001	03782	103-2103-001
	ATTENUATORS			
AT1 thru AT4	20 dB, 50 Ω	151-3002-001	23223	50102043-01-07C
A6A2	ATTENUATOR 70 dB	103-3044-001	03782	103-3044-001
	DIODES			
CR1 thru CR8	Switching, MF, 10 mA, 75 V	154-3001-001	IND-STD	1N4454
A6A2A1	COVER & FILTER	103-2095-001	03782	103-2095-001
A6A2A1A1	PHOTOXSTOR	103-1847-001	03782	103-1847-001
	TRANSISTOR			
PT1 thru PT3	Photo NPN	153-8001-001	07263	FPT100
Q1 thru Q3	NPN, Silicon, 20 VC Max, 500 mW, B60-1000	153-3009-001	IND-STD	2N5133
Q4 thru Q9	Difused Silicon, 30 VC Max, 500 mW, B150-300	556-147-059	IND-STD	2N4916
	RESISTORS			
R1 thru R3	62 KΩ, ±5%, 1/4W, Comp.	151-1002-623J	19701	CR25-1-4-5P-62K

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A6A2A1A1	(Cont.)			
R4 thru R6	1.8 KΩ, ±5%, 1/4 W, Comp.	151-1002-182J	19701	CR25-1-4-5P-1.8K
R7 thru R9	1.5 KΩ, ±5%, 1/4 W, Comp.	151-1002-152J	19701	CR25-1-4-5P-1.5K
A6A2A1A2	LAMP	103-1846-001	03782	103-1846-001
	INDICATORS			
DS1 thru DS3	Lamp, .04 A, 6.3 V	160-6007-001	71744	2180
	RESISTORS			
R1 thru R3	22 Ω, ±5%, 1/4 W, Comp.	151-1002-220J	19701	CR25-1-4-5P-22Ω
A6A2A1A3	FILTER CASE	103-1934-001	03782	103-1934-001
	CAPACITOR			
C8	8500 pF, GMV, 500 V, fixed cer.	150-1013-001	00656	BLF-1CC/852Z
A6A2A1A3A1	RFI FILTER	103-1852-001	03782	103-1852-001
	CAPACITORS			
	NOTE: Unless otherwise specified, all capacitors are fixed ceramic.			
C1	8500 pF, GMV, 500 V	150-1013-001	00656	BLF-1CC/852Z
C2	.47 µF, ±20%, 25 V	556-120-160	56289	5C023474X0250B3
C3	1000 pF, GMV, 500 V, FT	556-005-381	01121	FA5C/102W
C4	.47 µF, ±20%, 25 V	556-120-160	56289	5C023474X0250B3
C5	1000 pF, GMV, 500 V, FT	556-005-381	01121	FA5C/102W
C6, C7	.47 µF, ±20%, 25 V	556-120-160	56289	5C023474X0250B3
	INDUCTORS			
L1	Choke 750 Ω/50 MHz, ±20%	156-7005-002	02114	VK200 10/3B
L2	30 Turns, #30 Wire on closed Ferrite Core	132-0382-001	03782	132-0382-001
L3	Choke 750 Ω/50 MHz, ±20%	156-7005-002	02114	VK200 10/3B
L4	30 Turns, #30 Wire on closed Ferrite Core	132-0382-001	03782	132-0382-001
L5	Choke 750 Ω/50 MHz, ±20%	156-7005-002	02114	VK200 10/3B
L6	30 Turns, #30 Wire on closed Ferrite Core	132-0382-001	03782	132-0382-001

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A6A2A2	70 dB ATTENUATOR & MTG PLATE	103-2099-001	03782	103-2099-001
AT1	10 dB, 50 Ω	151-3001-001	23223	50102079-01-07C
AT2 thru AT4	20 dB, 50 Ω	151-3002-001	23223	50102043-01-07C
A7	SWITCH & MODULATOR	103-3034-001	03782	103-3034-001
	INTEGRATED CIRCUITS			
A1 thru A3	Hi Performance Op. Amp	84-1	18324	LM101A
A4 thru A6	DC Amp	153-7005-001	07263	UA702C/U5B7702393
A7	Hi Performance Op. Amp	84-1	18324	LM101A
	CAPACITORS			
	NOTE: Unless otherwise specified, all capacitors are fixed ceramic.			
C1, C2	50 µF, +75-10%, 50 V, Elec.	150-5001-500DS	56289	30D506G050DD2
C3	10 µF, +75-10%, 15 V, Elec.	150-5001-100DS	56289	30D106G015BA2
C4	35 µF, +75-10%, 15 V, Elec.	150-5001-350DS	56289	30D356G015CB2
C5	100 µF, +75-10%, 6 V, Elec.	150-5001-101BS	56289	30D107G006CC2
C6	120 pF, ±2%, 500 V, DM	150-2002-121FG0	72136	CD15FD121G03
C7	33 µF, ±20%, 25 V, Elec.	13-91	56289	196D336X0025LA3
C8	1 µF, ±20%, 50 V	12-94	72982	8131-M050-651-105M
C9, C10	0.01 µF, ±2%, 200 V, Mylar	14-26	18489	VT103H2A
C11	120 pF, ±2%, 500 V, DM	150-2002-121FG0	72136	CD15FD121G03
C12, C13	0.1 µF, ±2%, 200 V, PL	14-25	18489	VT104H2A
C14	120 pF, ±2%, 500 V, DM	150-2002-121	72136	CD15FD121G03
C15 thru C17	2.2 µF, ±20%, 100 V	12-81	72982	8151-100-651-225M
C18	1000 pF, ±2%, 100 V, DM	150-2002-102FG0	72136	CD15FA102G03
C19	.01 µF, ±10%, 100 V	12-88	72982	8121-100-W5R-103K
C20	62 pF, ±2%, 500 V, DM	150-2002-620EG0	72136	CD15ED620G03
C21	.01 µF, ±10%, 100 V	12-88	72982	8121-100-W5R-103K
C22	47 pF, ±2%, 500 V, DM	150-2002-470EG0	14655	CD15ED470G03
C23	5 µF, +75-10%, 25 V, Elect.	150-5001-5R0FS	56289	30D505G025BA2

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A7	(Cont.)			
C24	1000 pF, ±2%, 100 V, DM	150-2002-102FG0	72136	CD15FA102G03
C25, C26	.01 µF, ±10%, 100 V	12-88	72982	8121-100-W5R-103K
C27	100 pF, ±2%, 500 V, DM	150-2002-101FG0	14655	CD15FD101G03
C28	10 µF, ±20%, 63 V, PL	556-146-920	25088	B32110C9106M
C29	1000 pF, ±2%, 1000 V, DM	150-2002-102FG0	72136	CD15FA102G03
C30	.01 µF, ±10%, 100 V	12-88	72982	8121-100-W5R-103K
C31	100 pF, ±2%, 500 V, DM	150-2002-101FG0	14655	CD15FD101G03
C32	.01 µF, ±10%, 100 V	12-88	72982	8121-100-W5R-103K
C33	150 pF, ±2%, 500 V, DM	150-2002-151FG0	72136	DM15F151G0
C34	.01 µF, ±10%, 100 V	12-88	72982	8121-100-W5R-103K
C35	1 µF, ±20%, 50 V	12-94	72982	8131-M050-651-105M
C36	Factory Selected			
C37	.01 µF, ±10%, 100 V	12-88	72982	8121-100-W5R-103K
C38, C39	0.1 µF, ±20%, 100 V	12-72	72982	8131-100-W5R-104M
C40	56 pF, ±2%, 500 V, DM	150-2002-560EG0	72136	DM15E560G0
C41	2.2 µF, 35 V, Elec.	556-146-506	06751	CS 13 BF225K
C42	10 pF, ±5%, 500 V, DM	150-2002-100CJ0	IND-STD	CM05CD100J03
	DIODES			
CR1	G.P., 200 mA, 80 V	81-90	IND-STD	1N270
CR2 thru CR9	G.P., 10 mA, 75 V	154-0013-001	IND-STD	1N4148
CR10	Hot Carrier, 70 V, 250 mW	154-4001-001	07263	5082-2800
CR11	G.P., 10 mA, 75 V	154-0013-001	IND-STD	1N4148
CR12	Zenor, 5.0 V, 1.0 W	81-301	IND-STD	1N4742A
CR13	G.P., 10 mA, 75 V	154-0013-001	IND-STD	1N4148
	INDICATOR			
DS1	Lamp, 14 V, .080 A	160-6012-001	08730	VM2616
	TRANSISTORS			
Q1	NPN, Silicon, 20 VC Max, 500 mW, B60-1000	153-3009-001	IND-STD	2N5133
Q2	FET, 1 K µmhos, 40 V, P Channel	153-3012-001	IND-STD	2N5460

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A7	(Cont.)			
Q3, Q4	40 VC Max, 0.8 W, B150-750	81-267	IND-STD	2N5255
Q5	NOT ASSIGNED			
Q6	30 VC, 0.35 W, B100-300	153-3011-001	IND-STD	2N3643
	RESISTORS			
	NOTE: Unless otherwise specified all resistors are fixed 1/4 W, ±1% metal film.			
R1	1.40 KΩ	59-1.40K	19701	RN55-D-1401F
R2	NOT ASSIGNED			
R3	2.1 KΩ	59-2.10K	19701	MF5C-D-2101F
R4	392 Ω	59-392	19701	MF5C-D-3920F
R5	619 Ω	59-619	19701	RN55-D-6190F
R6	1.82 KΩ	59-1.82K	19701	MF5C-D-1821F
R7	33.2 KΩ	59-33.2K	19701	RN55-D-3322F
R8	18.2 KΩ	59-18.2K	19701	MF5C-D-1822F
R9	5.62 KΩ	59-562	19701	RN55-D-5621F
R10	365 Ω	59-365	19701	RN55-D-3650F
R11	392 K	59-392K	19701	RN55-D-3923F
R12	1.82 KΩ	59-1.82K	19701	MF5C-D-1821F
R13	6.04 KΩ	59-6.04K	19701	RN55-D-6042F
R14	5 KΩ, ±10%, 3/4 W, Trim PC	71-94	75042	960-290-5KΩ
R15	18.7 KΩ	59-18.7K	19701	RN55-D-1872F
R16	178 KΩ	59-178K	19701	MF5C-D-1783F
R17	49.9 K	59-49.9K	19701	MF5C-D-4992F
R18	6.65 KΩ	59-6.65K	19701	RN55-D-6651F
R19	16.5 KΩ	59-16.5K	19701	RN55-D-1652F
R20	1.50 KΩ	59-1.50K	19701	MF5C-D-1501F
R21	1 KΩ	59-1.00K	19701	MF5C-D-1001F
R22	5 KΩ, ±10%, 3/4 W, Trim PC	71-94	75942	960-290-5KΩ
R23	20 K, 1/2 W, Trim PC	71-146	75042	960-290-20K
R24	31.6 KΩ	59-31.6K	19701	RN55-D-3162F

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A7	(Cont.)			
R25, R26	1 KΩ	59-1.00K	19701	MF5C-D-1001F
R27	10.0 KΩ	59-10.0K	19701	RN55-D-1002F
R28 thru R30	100 KΩ	59-100K	19701	MF5C-D-1003F
R31	4.75 KΩ	59-4.75K	19701	RN55-D-4751F
R32	806 Ω	59-806	19701	RN55-D-8060F
R33	13.7 KΩ	59-13.7K	19701	RN55-D-1372F
R34	14.7 KΩ	59-14.7K	19701	RN55-D-1472F
R35	866 Ω	59-866	19701	MF5C-D-8660F
R36	464 Ω	59-464	19701	RN55-D-4640F
R37, R38	10.0 KΩ	59-10.0K	19701	RN55-D-1002F
R39	15.8 KΩ	59-15.8K	19701	RN55-D-1582F
R40, R41	162 Ω	59-162	19701	RN55-D-1620F
R42, R43	100 Ω	59-100	19701	MF5C-D-1000F
R44	1 KΩ	59-1.00K	19701	MF5C-D-1001F
R45	100 Ω	59-100	19701	MF5C-D-1000F
R46 thru R48	2 KΩ	59-2.00K	19701	MF5C-D-2001F
R49	10.0 KΩ	59-10.0K	19701	RN55-D-1002F
R50	205 Ω	59-205	19701	RN55-D-2050F
R51	1.50 KΩ	59-1.50 K	19701	MF5C-D-1501F
R52	15 Ω	59-15.0	19701	RN55-D-1500F
R53	750 Ω, 1/2 W	56-750	19701	MF6C-D-7500F
R54	15 Ω	59-15.0	19701	RN55-D-1500F
R55	121 KΩ	59-121K	19701	RN55-D-1213F
R56	10 KΩ, 1/2 W	56-10.0K	19701	MF6C-D-1000F
R57	121 KΩ	59-121K	19701	RN55-D-1213F
R58	5.11 KΩ	59-5.11K	19701	RN55-D-5111F
R59	38.3 K	59-38.3K	19701	RN55-D-3832F
R60	2.43 KΩ	59-2.43K	19701	MF5C-D-2431F

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A7	(Cont.)			
R61	10 Ω	59-10.0	19701	MF5C-D-10R0F
R62	2.43 KΩ	59-2.43K	19701	MF5C-D-2431F
R63	2 KΩ	59-2.00K	19701	MF5C-D-2001F
R64	205 Ω	59-205	19701	RN55-D-2050F
R65	2 KΩ	59-2.00K	19701	MF5C-D-2001F
R66	158 Ω	59-158K	19701	RN55-D-1580F
R67	10.0K Ω	59-10.0K	19701	RN55-D-1002F
R68	21.0 KΩ	59-21.0K	19701	RN55-D-2102F
R69, R70	205 Ω	59-205	19701	RN55-D-2050F
R71	10.0 KΩ	59-10.0K	19701	RN55-D-1002F
R72	20 K, 1/2 W, Trim PC	71-146	75942	960-290-20K
R73	Factory Selected			
R74	976 K	59-976K	19701	RN60-D-9763F
R75	511 Ω	59-511	19701	MF5C-D-5110F
R76	4.99 KΩ	59-4.99K	19701	MF5C-D-4991F
R77	10 KΩ, ±10%, 3/4 W Trimpot	71-93	75042	960-290-10K
R78	20.0 KΩ	59-20.0K	19701	MF5C-D-2002F
R79	49.9 K	59-49.9K	19701	MF5C-D-4992F
R80	500 Ω, ±10%, 3/4 W	71-91	75042	960-20-500Ω
R81	1.50 KΩ	59-1.50K	19701	MF5C-D-1501F
R82	976 K	59-976K	19701	RN60-D-9763F
R83	10.0 KΩ	59-10.0K	19701	RN55-D-1002F
R84	NOT ASSIGNED			
R85	6.81 KΩ	59-6.81K	19701	MF5C-D-6811F
R86	12.1 KΩ	59-12.1K	19701	RN55-D-1212F
R87	2.43 KΩ	59-24.3K	19701	RN55-D-2431F
R88	1 KΩ	59-1.00K	19701	MF5C-D-1001F
R89	Factory Selected			

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A7	(Cont.)			
	SWITCHES			
S1 thru S10	Push Bottom	161-0023-001	85514	F/B 009-262
A7A1	PUSH BUTTON ASSEMBLY	103-3041-001	03782	103-3041-001
A8	COUNTER ASSEMBLY	103-2163-001	03782	103-2163-001
A8A1	FILTER/COVER	103-3039-001	03782	103-3039-001
	FILTERS			
FL1 thru FL7	Pi Circuit, 0.1 A	156-9011-001	56289	1JX2703
FL8	Pi Circuit	156-9012-001	56289	3JX2331
FL9	Pi Circuit, 0.1 A	156-9011-001	56289	1JX2703
FL10	Pi Circuit	156-9012-001	56289	3JX2331
FL 11 thru FL 13	Cap. Cer. .005 µF, 200 V, FT	12-83	33095	51-719-021
A8A2	DAUGHTER BOARD	103-3037-001	03782	103-3037-001
A8A3	MOTHER BOARD	103-3085-001	03782	103-3085-001
	CONNECTORS			
J1	Mod 20 Pin	149-0237-001	03782	149-0237-001
J2, J3	Mod 38 Pin	149-0236-001	03782	149-0236-001
J4	Mod 20 Pin	149-0237-001	03782	149-0237-001
J5	Mod 38 Pin	149-0236-001	03782	149-0236-001
J6, J7	Mod 20 Pin	149-0237-001	03782	149-0237-001
	RELAY			
K1	6 V, 325 Ω coil	158-0005-001	29750	2275/6V
A8A3A2	DISPLAY	103-2143-001	03782	103-2143-001
	CAPACITORS			
C1 thru C6	.1 µF, ±20%, 25 V, Fixed Cer.	556-120-162	56289	5C023104X0250B3
	INDICATORS			
DS1, DS2	Lamp, 5V, Miniature 3/4 Amp	160-6009-001	10133	GMW 3/4 A

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A8A3A2	(Cont.)			
	INTEGRATED CIRCUITS			
IC1	Light Emit Diode Array	153-7046-001	01295	OPCOA SLA-1
IC2	BCD to 7 Bit Decoder	153-7032-001	18324	S7447A
IC3	Light Emit Diode Array	153-7046-001	01295	OPCOA SLA-1
IC4	BCD to 7 Bit Decoder	153-7032-001	18324	S7447A
IC5	Light Emit Diode Array	153-7046-001	01295	OPCOA SLA-1
IC6	BCD to 7 Bit Decoder	153-7032-001	18324	S7447A
IC7	Light Emit Diode Array	153-7046-001	01295	OPCOA SLA-1
IC8	BCD to 7 Bit Decoder	153-7032-001	18324	S7447A
IC9	Light Emit Diode Array	153-7046-001	01295	OPCOA SLA-1
IC10	BCD to 7 Bit Decoder	153-7032-001	18324	S7447A
IC11	Light Emit Diode Array	153-7046-001	01295	OPCOA SLA-1
IC12	BCD to 7 Bit Decoder	153-7032-001	18324	S7447A
IC13	Quad. 2-Input Nand Buffer	153-7030-001	18324	S5437A
IC14	Quad. 2-Input Nand Gates	153-7031-001	01295	SN5400N
	RESISTORS			
	NOTE: Unless otherwise specified, all resistors are fixed comp. 1/4 W, ±5%.			
R1, R2	150 Ω	151-1002-151J	12987	RC07GF151J
R3, R4	2 KΩ, 1/8 W	151-1016-202J	19701	CR16-1-8-5P-2K
R5, R6	15 Ω	151-1002-150J	12987	RC07GF150J
R7 thru R52	200 Ω, 1/8 W	151-1016-201J	19701	CR16-1-8-5P-200Ω
A8A3A3	STORAGE/COUNTER	103-3029-001	03782	103-3029-001
	CAPACITORS			
C1 thru C5	.1 μF, ±20%, 25 V, fixed cer.	556-120-162	56289	5C023104X0250B3
	INTEGRATED CIRCUITS			
IC1 thru IC6	Synchronous 4-Bit Up/Down Counters	153-7050-001	18324	S54192A
IC7 thru IC12	8-Bit and 4-Bit Bistable Latches	153-7034-001	18324	S5475B

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A8A3A3	(Cont.)			
IC13	Quad. 2-Input Nand Gates	153-7031-001	01295	SN5400N
IC14 thru IC16	Dual 4-Input Nor Gates With Strobe	153-7048-001	01295	SN5425N
IC17	8-Input Nand Gates	153-7049-001	18324	S5430A
IC18	Monostable Multivibrator	153-7044-001	01295	SN5412IN
IC19	Dual D-Type Edge-Triggered Flip-Flops	153-7040-001	18324	S54H74A
	RESISTORS			
R1 thru R4	2 K, ±5%, 1/4 W, comp.	151-1002-202J	19701	CR25-1-4-5P-2K
R5	15 K, ±5%, 1/4 W, comp.	151-1002-153J	19701	CR25-1-4-5P-15K
A8A3A4	PRE SCALER	103-3031-001	03782	103-3031-001
	CAPACITORS			
	NOTE: Unless otherwise specified, all capacitors are fixed ceramic.			
C1	0.01 µF, ±20%, 25 V	12-56	56289	C069B250E103Z
C2, C3	1 µF, ±20%, 50 V	12-94	72982	8131-M050-651-105M
C4	Factory Selected			
C5	1 µF, ± 20%, 50 V	12-94	72982	8131-M050-651-105M
C6 thru C9	0.1 µF, ±20%, 100 V	12-72	72982	8131-100-W5R-104M
C10	.001 µF, ±10%, 1000 V	12-2	72982	851-X5R-102K
C11	1 µF, ±20%, 50 V	12-94	72982	8131-M050-651-105M
	DIODES			
CR1, CR2	Switching, MF, 10 mA, 75 V	154-3001-001	IND-STD	IN4454
	INTEGRATED CIRCUITS			
IC1 thru IC3	Dual D-Type Edge-Triggered Flip-Flops	153-7040-001	18324	S54H74A
IC4	Expandable Dual 2-Wide 2-Input and/or Invert Gates	153-7039-001	18324	S5450A
IC5	Hex Inverters	153-7035-001	18324	S5404A
IC6	Quad. 2-Input Nor Gate	153-7041-001	18324	S5402A
IC7	Dual 2 Wide 2 Input Nand/Nor Gate	153-7038-001	18324	S5453A
IC8, IC9	Quad 2-Input Nand Gates	153-7031-001	01295	SN5400N

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A8A3A4	(Cont.)			
IC10	Quad 2-Input Nand Buffer	153-7030-001	18324	S5437A
IC11	Expandable Dual 2-Wide 2-Input and/or Invert Gates	153-7039-001	18324	S5450A
	TRANSISTORS			
Q1	10 VC Max, 200 mW, B20-150	81-215	IND-STD	2N5134
Q2, Q3	40 VC Max, 0.31 mW, B100-300	556-146-989	IND-STD	2N3904
Q4	50 VC Max, 310 mW, B250-800	153-3028-001	IND-STD	2N5087
	RESISTORS			
	NOTE: Unless otherwise specified, all resistors are fixed comp. 1/4 W, ±5%.			
R1	220 Ω	151-1002-221J	19701	CR25-1-4-5P-220Ω
R2	75 KΩ	151-1002-753J	19701	CR25-1-4-5P-75K
R3	1 KΩ	151-1002-102J	19701	CR25-1-4-5P-1K
R4 thru R6	2 K	151-1002-202J	19701	CR25-1-4-5P-2K
R7, R8	22 KΩ	151-1002-223J	19701	CR25-1-4-5P-22K
R9	3.9 K	151-1002-392J	19701	CR25-1-4-5P-3.9K
R10	220 Ω	151-1002-221J	19701	CR25-1-4-5P-220Ω
R11	24 K	151-1002-243J	19701	CR25-1-4-5P-24K
R12	4.7 K	151-1002-472J	19701	CR25-1-4-5P-4.7K
R13	3300 Ω	151-1002-332J	19701	CR25-1-4-5P-3.3K
R14	240 Ω	151-1002-241J	19701	CR25-1-4-5P-240Ω
R15	470 KΩ	151-1002-474J	19701	CR25-1-4-5P-470K
R16	47 KΩ	151-1002-473J	19701	CR25-1-4-5P-47K
R17	10 KΩ	151-1002-103J	19701	CR25-1-4-5P-10K
R18	470 Ω	151-1002-471J	19701	CR25-1-4-5P-470Ω
R19	10 KΩ	151-1002-103J	19701	CR25-1-4-5P-10K
R20	4.7 K	151-1002-472J	19701	CR25-1-4-5P-4.7K
R21	47 Ω	151-1002-470J	19701	CR25-1-4-5P-47Ω
A8A3A5	TIME BASE	103-3030-001	03782	103-3030-001

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A8A3A5	(Cont.)			
C1 thru C3	.1 µF, ±20%, 25 V, fixed cer.	556-120-162	56289	5C023104X0250B3
C4	1 µF, ±20%, 50 V, fixed cer.	12-94	72982	8131-M050-641-105M
C5	33 pK, ±2%, 500 V, fixed DM	150-2002-330EG0	14655	CD15ED330G03
C6	20 pF, ±2%, 500 V, fixed DM	150-2002-200EG0	14655	CD15CD200G03
C7	1 µF, ±20%, 50 V, fixed cer.	12-94	72982	8131-M050-651-105M
	DIODE			
CR1	Switching, MF, 10 mA, 75 V	154-3001-001	IND-STD	IN4454
	INTEGRATED CIRCUITS			
IC1	Hex Inverters	153-7035-001	18324	S5404A
IC2	Expandable Dual 2-Wide 2-Input and/or Invert Gates	153-7039-001	18324	S5450A
IC3	Dual Flip Flop	153-7036-001	18324	S54107A
IC4	Quad. 2-Input Nand Gates	153-7031-001	01295	SN5400N
IC5	Dual D-Type Edge-Triggered Flip-Flops	153-7040-001	18324	S54H74A
IC6 thru IC9	Decade Counters	153-7033-001	18324	S5490A
IC10	Dual 4/1 Line Parallel/Serial Converter	153-7047-001	01295	SN54153N
IC11, IC12	Decade Counters	153-7033-001	18324	S5490A
IC13 thru IC15	Dual Flip Flop	153-7036-001	18324	S54107A
IC16	Triple 3-Input Nand Gates	153-7037-001	18324	S5410A
IC17	Quad. 2-Input Nand Buffer	153-7030-001	18324	S5437A
	TRANSISTORS			
Q1	30 VC Max., 310 mW, B300-900	81-195	04713	2N5088
Q2	50 VC Max., 310 mW, B250-800	153-3028-001	IND-STD	2N5087
	RESISTORS			
	NOTE: Unless otherwise specified, all resistors are fixed comp. 1/4 W, ±5%.			
R1	2 K	151-1002-202J	19701	CR25-1-4-5P-2K
R2	10 KΩ	151-1002-103J	19701	CR25-1-4-5P-10K
R3	47 KΩ	151-1002-473J	19701	CR25-1-4-5P-47K

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A8A3A5	(Cont.)			
R4	10 KΩ	151-1002-103J	19701	CR25-1-4-5P-10K
R5	2.2 K	151-1002-222J	19701	CR25-1-4-5P-2.2K
R6	220 Ω	151-1002-221J	19701	CR25-1-4-5P-220Ω
R7	470 KΩ	151-1002-474J	19701	CR25-1-4-5P-470K
R8	12 KΩ	151-1002-123J	19701	CR25-1-4-5P-12K
R9, R10	10 KΩ	151-1002-103J	19701	CR25-1-4-5P-10K
R11	470 Ω	151-1002-471J	19701	CR25-1-4-5P-470Ω
R12 thru R15	2 KΩ	151-1002-202J	19701	CR25-1-4-5P-2K
A8A3A6	OSCILLATOR	103-2147-001	03782	103-2147-001
	CAPACITORS			
	NOTE: Unless otherwise specified, all capacitors are fixed ceramic.			
C1	.1 µF, ±20%, 25 V	556-120-162	56289	5C023104X0250B3
C2	1 µF, ±20%, 50 V	12-94	72982	8131-M050-651-105M
C3	91 pF, ±2%, 500 V, DM	150-2002-910FG0	72136	DM15F910G0500
C4	Factory Selected			
C5, C6	.1 µF, ±20%, 25 V	556-120-162	56289	5C023104X0250B3
C7	5.6 µF, ±20%, 35 V, Tant.	13-88	56289	150D565X903B2
C8	1-20 pF, 250 V, Var.	150-0016-001	91293	JMC-5501
C9	330 pF, ±2%, 500 V, DM	150-2002-331FG0	72136	DM15F331G0500
C10	.01 µF, ± 10%, 150 V	150-1034-001	72982	8141-M100-C0G-103K
C11	.1 µF, ±20%, 25 V	556-120-162	56289	5C023104X0250B3
C12 thru C14	.01 µF, ± 10%, 150 V	150-1034-001	72982	8141-M100-C0G-103K
C15	.1 µF, ±20%, 25 V	556-120-162	56289	5C023104X0250B3
C16	.01 µF, ± 10%, 150 V	150-1034-001	72982	8141-M100-C0G-103K
C17	6 pF, ±.25 pF, 500 V	150-1012-060CC	IND-STD	CC20CH060C
C18	68 pF, ±2%, 500 V, DM	150-2002-680	14655	CD15ED680G03
C19	.01 µF, ± 10%, 150 V	150-1034-001	72982	8141-M100-C0G-103K
C20	39 pF, ±2%, 500 V, DM	150-2002-390EG0	72136	CD15ED390G03

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A8A3A6	(Cont.)			
	DIODES			
CR1 thru CR4	Switching, MF, 10 mA, 75V	154-3001-001	IND-STD	IN4454
	INTEGRATED CIRCUITS			
IC1	Hex Inverter	153-7043-001	18324	S5405A
IC2	Expandable Dual 2-Wide 2-Input and/or Invert Gates	153-7039-001	18324	SN5450N
IC3	Monostable Multivibrator	153-7044-001	01295	SN5412IN
IC4	Dual D-Type Edge-Triggered Flip-Flops	153-7040-001	18324	S54H74A
	INDUCTOR			
L1	5.6 μH/1.15 Ω, ±10%	556-012-094	99848	WD56G
	TRANSISTORS			
Q1, Q2	NPN, Silicon, 20 VC Max, 500 mW, B60-1000	153-3009-001	IND-STD	2N5133
Q3	Difused Silicon, 30 VC Max, 500 mW, B150-300	556-147-059	IND-STD	2N4916
Q4, Q5	NPN, Silicon, 18 VC Max, 500 mW, B75-min.	153-3003-001	IND-STD	2N5183
Q6 thru Q8	12 VC Max, 200 mW, B30-500	153-3008-001	IND-STD	2N5130
	RESISTORS			
	NOTE: Unless otherwise specified, all resistors are fixed comp. 1/4 W, ±5%.			
R1	Res Trim PC, 500 Ω, ±20%	556-203-010	23223	X201R501B
R2	Res Trim PC, 1K, ±20%	556-056-124	23223	X201R-102B
R3, R4	1 KΩ	151-1002-102J	19701	CR25-1-4-5P-1K
R5	1.8 KΩ	151-1002-182J	19701	CR25-1-4-5P-1.8K
R6	10 KΩ	151-1002-103J	19701	CR25-1-4-5P-10K
R7	1 KΩ	151-1002-102J	19701	CR25-1-4-5P-1K
R8	750Ω	151-1002-751J	19701	CR25-1-4-5P-750Ω
R9	3.6 K	151-1002-362J	19701	CR25-1-4-5P-3.6K
R10	4.7K	151-1002-472J	19701	CR25-1-4-5P-4.7K
R11	10 KΩ	151-1002-103J	19701	CR25-1-4-5P-10K
R12	3 KΩ	151-1002-302J	19701	CR25-1-4-5P-3K
R13	2.7 K	151-1002-272J	19701	CR25-1-4-5P-2.7K

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A8A3A6	(Cont.)			
R14	510 Ω	151-1002-511J	19701	CR25-1-4-5P-510Ω
R15	2 K	151-1002-202J	19701	CR25-1-4-5P-2K
R16 thru R19	6.8 KΩ	151-1002-682J	19701	CR25-1-4-5P-6.8K
R20	220 Ω	151-1002-221J	19701	CR25-1-4-5P-220Ω
R21	2 K	151-1002-202J	19701	CR25-1-4-5P-2K
R22	510 Ω	151-1002-511J	19701	CR25-1-4-5P-510Ω
R23	220 Ω	151-1002-221J	19701	CR25-1-4-5P-220Ω
R24	2.7 K	151-1002-272J	19701	CR25-1-4-5P-2.7K
R25	2 K	151-1002-202J	19701	CR25-1-4-5P-2K
R26	560 Ω	151-1002-561J	19701	CR25-1-4-5P-560Ω
R27	7.87 KΩ, ±1% MF	59-7.87K	19701	RN55-D-7871F
R28	2.61 KΩ, ±1% MF	59-2.61K	19701	RN55-D-3611F
R29	6.8 KΩ	151-1002-682J	19701	CR25-1-4-5P-6.8K
R30	33 Ω	151-1002-330J	19701	CR25-1-4-5P-33Ω
R31	6.2 K	151-1002-622J	19701	CR25-1-4-5P-6.2K
R32	2.2K	151-1002-222J	19701	CR25-1-4-5P-2.2K
R33	220 Ω	151-1002-221J	19701	CR25-1-4-5P-220Ω
R34	2.2 K	151-1002-222J	19701	CR25-1-4-5P-2.2K
R35	82 K	151-1002-823J	19701	CR25-1-4-5P-82K
R36	4.7 K	151-1002-472J	19701	CR25-1-4-5P-4.7K
R37	1 KΩ, ±1% MF	59-1.00K	19701	MF5C-D-1001F
R38	3.57 KΩ, ±1% MF	59-3.57K	19701	RN55-D-3571F
	CRYSTAL			
Y1	Glass Case 4 MHz	155-0008-001	33096	PB-1083
A8A3A7	AFC	103-3035-001	03782	103-3035-001
	CAPACITORS			
C1	100 pF, ±2%, 500 V, DM	150-2002-220EG0	72136	DM15E220G0
C2	2.2 µF, 35 V, Tant.	556-146-506	06751	CS 13 BF 225K
C3	.33 µF, ±10%, 80 V, PL	14-51	56289	192P3349R8

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A8A3A7	(Cont.)			
C4	NOT ASSIGNED			
C5	0.1 µF, ±2%, 200 V, PL	14-25	18489	VT104H2A
C6	50 µF, +75-10%, 25 V, Elec.	150-5001-500ES	14655	NLW-50-25
C7	100 pF, ±2%, 500 V, DM	150-2002-220EG0	72136	DM15E220G0
C8	NOT ASSIGNED			
C9	50 µF, +75-10%, 50 V, Elec.	150-5001-500FS	14655	NLW-50-50
C10	Factory Selected			
	DIODES			
CR1	Switching, MF, 10 mA, 75 V	154-3001-001	IND-STD	1N4454
CR2 thru CR11	NOT ASSIGNED			
CR12	Switching, MF, 10 mA, 75 V	154-3001-001	IND-STD	1N4454
	INDUCTOR			
L1	Choke 750 Ω/50 MHz, ±20%	156-7005-002	02114	VK200 10/3B
	TRANSISTORS			
Q1	Difused Silicon, 30 VC Max, 500 mW, B150-300	556-147-059	IND-STD	2N4916
Q2	FET 60-180 µmhos, 40 V p channel	153-3027-001	IND-STD	2N5471
Q3	Difused Silicon, 30 VC Max, 500 mW, B150-300	556-147-059	IND-STD	2N4916
Q4	FET 60-180 µmhos, 40 V p channel	153-3027-001	IND-STD	2N5471
Q5, Q6	FET 1 K µmhos, 40 V p channel	153-3012-001	IND-STD	2N5460
Q7	Difused Silicon, 30 VC Max, 500 mW, B150-300	556-147-059	IND-STD	2N4916
	RESISTORS			
	NOTE: Unless otherwise specified, all resistors are fixed comp. 1/4 W, ±5%.			
R1	2 K	151-1002-202J	19701	CR25-1-4-5P-2K
R2	1.2 KΩ	151-1002-122J	19701	CR25-1-4-5P-1.2K
R3	27 KΩ	151-1002-273J	19701	CR25-1-4-5P-27K
R4	12 KΩ	151-1002-123J	19701	CR25-1-4-5P-12K
R5	100 KΩ	151-1002-104J	19701	CR25-1-4-5P-100K
R6	6.49 KΩ, ± 1%, MF	59-6.49K	19701	MF5C-D-6491F

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A8A3A7	(Cont.)			
R7	4.87 KΩ, ±1%, MF	59-4.87K	19701	RN55-D-4871F
R8	1.2 KΩ	151-1002-122J	19701	CR25-1-4-5P-1.2K
R9	27 KΩ	151-1002-273J	19701	CR25-1-4-5P-27K
R10	27.4 K, ±1%, MF	59-27.4 K	19701	MF5C-D-2742F
R11	2.43 KΩ, ±1%, MF	59-24.3K	19701	RN55-D-2431F
R12	1 M	151-1002-105J	81349	RC07GF105J
R13	100 KΩ	151-1002-104J	19701	CR25-1-4-5P-100K
R14	75 KΩ	151-1002-753J	19701	CR25-1-4-5P-75K
R15	10 KΩ	151-1002-103J	19701	CR25-1-4-5P-10K
R16	100 KΩ	151-1002-104J	19701	CR25-1-4-5P-100K
R17	1.2 KΩ	151-1002-122J	19701	CR25-1-4-5P-1.2K
R18, R19	27 KΩ	151-1002-273J	19701	CR25-1-4-5P-27K
R20	909 Ω, ±1%, MF	59-909	19701	RN55-D-9090F
R21	68 K	151-1002-683J	19701	CR25-1-4-5P-68K
	INTEGRATED CIRCUIT			
U1	Dual D-Type Edge-Triggered Flip-Flops	153-7040-001	18324	S54H74A
A9	POWER SUPPLY	103-3038-002	03782	103-3038-002
	CAPACITOR			
C1	36000 µF, 15 V, Elec.	150-5016-001	90201	CGS363U015U3L
	CONNECTOR			
J1	7 Contacts, 7.5 A, 2 KVAC, Female	133-9	81312	M7S-LRM
	TRANSISTORS			
Q1	60 VC Max, 87.5 W, B25-100	153-3021-001	IND-STD	2N4914
Q2, Q3	50 VC Max, 36 W, B30-120	153-5001-001	IND-STD	2N5296
Q4	40 VC Max, 87.5 W, B20-80	153-0018-001	IND-STD	2N4901
Q5	70 VC Max, 115 W, B20-70	153-0016-001	IND-STD	2N3055
	TRANSFORMER			
T1	Power	132-0445-001	17474	4-3068
A9A1	POWER SUPPLY	103-3027-001	03782	103-3027-001
	CAPACITORS			
C1	1100 µF, 50 V, Elec.	150-5010-009	56289	39D118G050HP4

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A9A1	(Cont.)			
C2	5400 µF, 25 V, Elec.	150-5017-001	53021	066JT542U025B
C3	8000 µF, 15-18 V, Elec.	556-201-100	56289	39D808G015JT4
	DIODES			
CR1, CR2	Silicon Rectifier 100 V, 22 A	154-1008-001	04713	MR 751
CR3, CR4	G.P. 10 W, 1A	81-20	IND-STD	IN4005
CR5, CR6	Bridge 50 V, 1.6A	154-1011-001	77638	W005
	CONNECTOR			
J1	38 Pin, .100 Cntrs-min. dip solder	168-3012-001	95238	600-121DD-19A
A9A2	POWER SUPPLY	103-3028-004	03782	103-3028-004
	CAPACITORS			
	NOTE: Unless otherwise specified, all capacitors are fixed ceramic.			
C1	5 µF, 50 V, Elec.	13-44	14655	NLW5-50
C2	0.1 µF, ±20%, 100 V	12-72	72982	8131-100-W5R-104M
C3	5 µF, 50 V, Elec.	13-44	14655	NLW5-50
C4	10 µF, 25 V, Elec.	150-5001-100ES	14655	NLW10-25
C5	10 µF, ±20%, 35 V, Elec.	12-82	88245	CY30A474M
C6, C7	0.1 µF, ±20%, 100 V	12-72	72982	8131-100-W5R-104M
C8	100 µF, 25 V, Elec.	150-5001-101ES	14655	NLW100-25
C9	30 pF, ±2%, 500 V, DM	150-2002-300EG0	72136	DM15E300G0500
C10	0.1 µF, ±20%, 100 V	12-72	72982	8131-100-W5R-104M
C11	30 pF, ±2%, 500 V, DM	150-2002-300EG0	72136	DM15E300G0500
C12, C13	0.1µF, ±20%, 100 V	12-72	72982	8131-100-W5R-104M
C14	100 µF, 15 V, Elec.	13-59	14655	NLW100-16
C15 thru C17	0.1 µF, ±20%, 100 V	12-72	72982	8131-100-W5R-104M
C18	62 pF, ±2%, 500 V, DM	150-2002-620EG0	72136	CD15ED620G03
C19	0.1 µF, ±20%, 100 V	12-72	72982	8131-100-W5R-104M
C20	100 µF, 15 V, Elec.	13-59	14655	NLW100-16

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A9A2	(Cont.)			
C21	30 pF, ±2%, 500 V, DM	150-2002-300EG0	72136	DM15E300G0500
C22 thru C24	0.1 µF, ±20 %, 100 V	12-72	72982	8131-100-W5R-104M
C25	100 µF, 15 V, Elec.	13-59	14655	NLW100-16
	DIODES			
CR1	Zener, 5.1 V, ±5%, 500 mW	154-2002-001	IND-STD	IN5231A
CR2	Zener, 12 V, ±5%, 1 W	81-301	IND-STD	IN4742A
CR3	Switching, MF, 10 mA, 75 V	154-3001-001	IND-STD	IN4454
CR4	Zener, 6.2 V, ±5%	154-0018-001	IND-STD	IN829A
CR5	Zener, 12 V, ±5%, 1W	81-301	IND-STD	IN4742A
CR6	Zener, 6.8 V, ±5%, 1 W	81-139	IND-STD	IN4736A
CR7, CR8	Switching, MF, 10 mA, 75 V	154-3001-001	IND-STD	IN4454
	INTEGRATED CIRCUITS			
IC1 thru IC4	Hi Performance Op. Amp.	84-1	18324	LM101A
	TRANSISTORS			
Q1	NOT ASSIGNED			
Q2	25 VC Max, 0.3 mW, B100-min.	81-114	07263	2N3638A
Q3A, Q3B	40 VC Max, 0.8 W, B150-750	81-267	IND-STD	2N5255
Q4	NOT ASSIGNED			
Q5	60 VC Max, 0.8 W, B40-120	153-0014-001	IND-STD	2N4030
Q6	NOT ASSIGNED			
Q7	30 VC Max, 0.8 W, B100-300	153-0015-001	IND-STD	2N2219
Q8	NPN, Silicon, 20 VC Max, 500 mW, B60-1000	153-3009-001	IND-STD	2N5133
Q9	NOT ASSIGNED			
Q10	60 VC Max, 0.8 W, B40-120	153-0014-001	IND-STD	2N4030
Q11	50 VC Max, 310 mW, B250-800	153-3028-001	IND-STD	2N5087
Q12 thru Q14	NOT ASSIGNED			
Q15	NPN, Silicon, 20 VC Max, 500 mW, B60-1000	153- 3009-001	IND-STD	2N5133
Q16	NOT ASSIGNED			

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A9A2	(Cont.)			
Q17	NPN, Silicon, 20 VC Max, 500 mW, B60-1000	153-3009-001	IND-STD	2N5133
	RESISTORS			
	NOTE: Unless otherwise specified, all resistors are fixed 1/4 W, ±1% metal film.			
R1, R2	1.5 K, ±5%, 1W Comp.	151-1004-152J	01121	CB1525
R3	47.5 KΩ	59-47.5K	19701	MF5C-D-4752F
R4	2.15 KΩ, 1/2 W	56-2.15K	19701	RN60-D-2151F
R5	3.65 KΩ	59-3.65K	19701	RN55-D-3651F
R6	2.94 KΩ	59-2.94K	19701	MF5C-D-2941F
R7	100 Ω, ±10%, 1W, Pot.	71-96	73138	79PR100
R8	953 Ω	59-953	19701	MF5C-D-9530F
R9	2.4 Ω, ±5%, 1/2 W, W-W	44-2.4Ω	75042	BWH-2.4Ω
R10	8.25 KΩ	59-8.25K	19701	MF5C-D-8251F
R11	22.1 KΩ	59-22.1K	19701	RN55-D-2212F
R12	470 Ω, ±5%, 1W, Comp.	151-1004-471J	MILPN	RC32GF471J
R13	2.26 KΩ	59-2.26K	19701	MF5C-D-2261F
R14	499 Ω	59-499	19701	MF5C-D-4990F
R15A, B	1.0 Ω, ±5%, 1/2 W, W-W	44-1.0Ω	75042	BWH-1.0Ω ±5%
R16	12.1 KΩ	59-12.1K	19701	RN55-D-1212F
R17	1 KΩ, ±10%, 3/4 W, Var, Trim	71-105	75042	960-20-1K
R18	25.5 K	59-25.5K	19701	RN55-D-2552F
R19	6.81 KΩ	59-6.81K	19701	MF5C-D-6811F
R20A, B	1.0 Ω, ±5%, 1/2 W, W-W	44-1.0Ω	75042	BWH-1.0Ω ±5%
R21	221 Ω	59-221	19701	RN55-D-2210F
R22	4.75 KΩ	59-4.75K	19701	MF5C-D-4751F
R23	1 KΩ, ±10%, 3/4 W, Var, Trim	71-105	75042	960-20-1K
R24	19.6K	59-19.6	19701	MF5C-D-1962F
R25	5.11 KΩ	59-5.11K	19701	RN55-D-5111F
R26	221 Ω	59-221	19701	RN55-D-2210F
R27A, B	.36 Ω, ±5%, 1/2 W, W-W	44-.36Ω	75042	BWH-.36Ω ±5%

CIRCUIT REFERENCE	DESCRIPTION	SINGER PART NO.	TRUE MFG. FSC NO.	TRUE MFG. PART NO.
A9A2	(Cont.)			
R28	2321 Ω	59-2.32K	19701	RN55-D-2321F
R29	500 Ω, ±10%, 3/4 W, ±100 ppm, 15 Turns, Trim PC	71-91	75042	960-20-500Ω
R30	13.0 KΩ	59-13.0K	19701	MF5C-D-1302F
R31	2.21 KΩ	59-2.21K	19701	MF5C-D-2211F
R32	1.5 Ω, ±5%, 2 W, W-W	44-1.5Ω	75042	BWH 1.5 Ω ±5%
R33	3.40 KΩ	59-3.40K	19701	MF5C-D-3401F
R34	6.19 KΩ	59-6.19K	19701	RN55-D-6191F
R35	1 KΩ, ±10%, 3/4 W, Var, Trim	71-105	75042	960-20-1K
R36	6.81 KΩ	59-6.81K	19701	MF5C-D-6811F
R37	10.0 KΩ	59-10.0K	19701	RN55-D-1002F
R38	1 KΩ	59-1.00K	19701	MF5C-D-1001F
A10	LOAD SIMULATOR	103-2054-001	03782	103-2054-001
	TRANSISTOR			
Q1	NPN, Silicon, 18 VC Max, 500 mW, B75-min.	153-3003-001	IND-STD	2N5183
	RESISTORS			
R1	20 KΩ, ±5%, 1/4 W, Comp.	151-2002-203J	19701	CR25-1-4-5P-20K
R2	8.2 K, ±5%, 1/4 W, Comp.	151-2002-822J	19701	CR25-1-4-5P-8.2K

SECTION VI

SUPPLEMENTARY SCHEMATIC DIAGRAMS

6-1. SUPPLEMENTARY SCHEMATICS BY MODULE RATHER THAN BY FUNCTION.

6-2. These schematics are included to help signal tracing, where signals may flow through several boards between two functional schematics. The paths are indicated, point by point, at entrance and exit terminals of the Functional Schematics in Section IV.

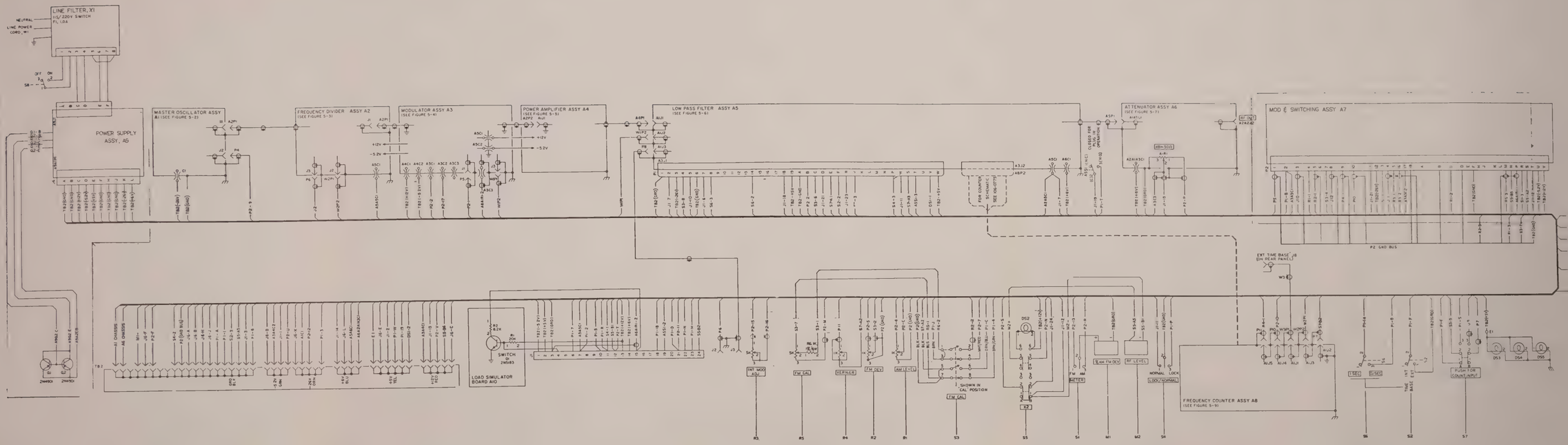
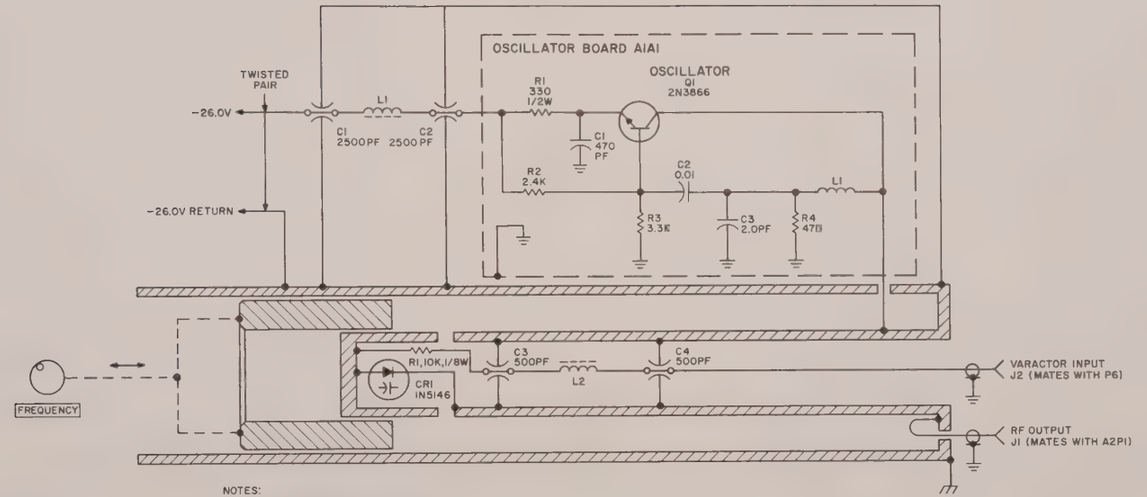


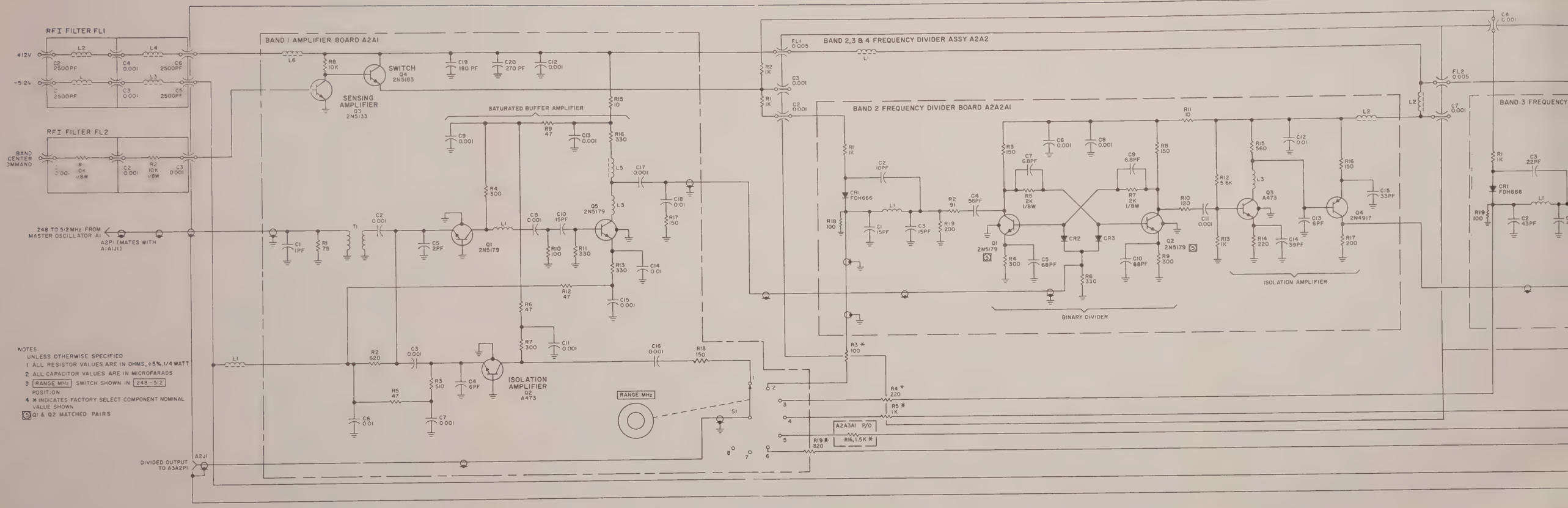
Figure 6-1. Wiring Diagram.

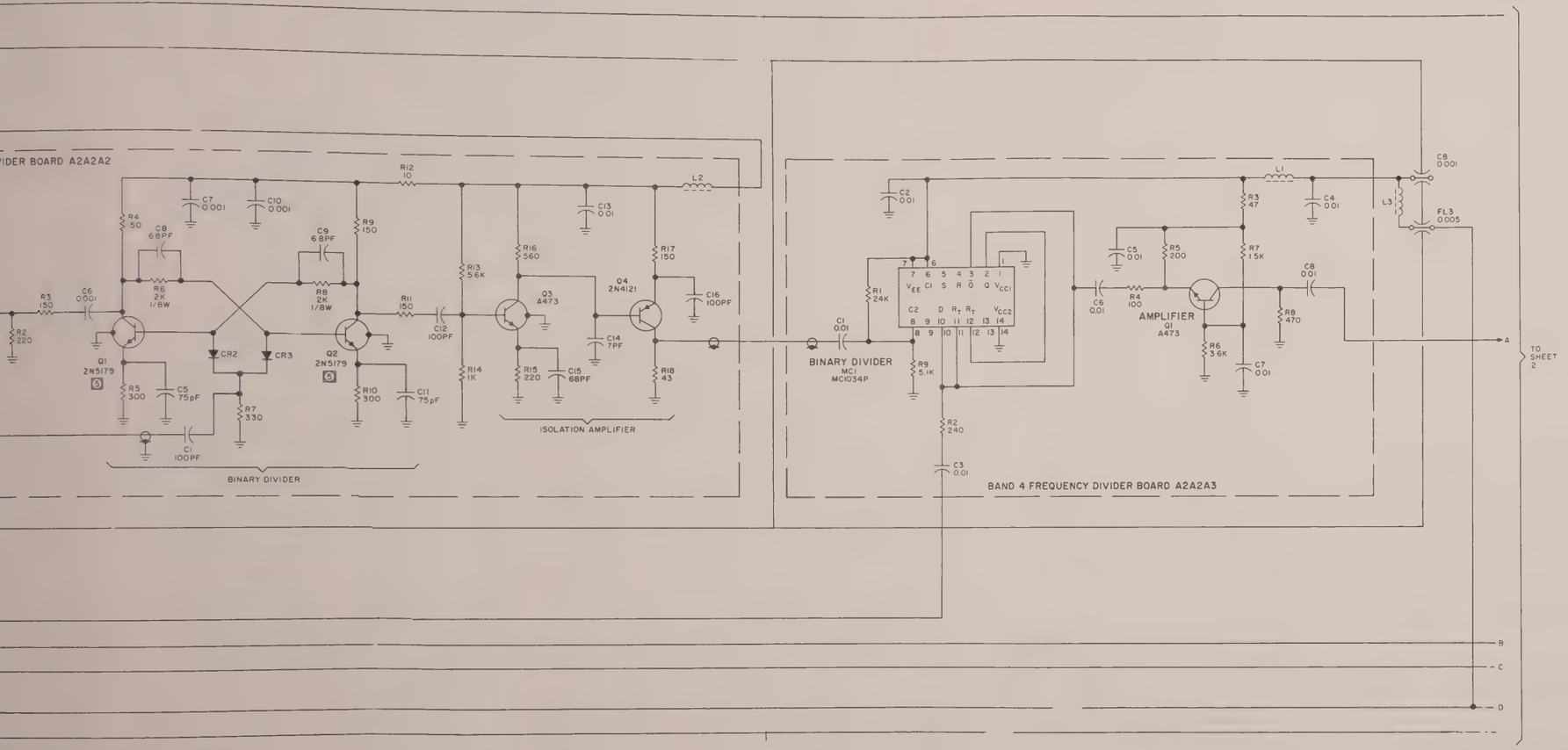


NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W
2. ALL CAPACITOR VALUES ARE IN MICROFARADS

6-2

Figure 6-2. Master Oscillator A1, Schematic Diagram.


RFI FILTER FL1
+12V
-5.2V
L2
L4
C2 2500PF
C4 0.001
C6 2500PF
L1
L3
C1 2500PF
C3 0.001
C5 2500PF
RFI FILTER FL2
BAND CENTER COMMAND
C1 0.001
R1 2K 1/8W
C2 0.001
R2 10K 1/8W
C3 0.001
248 TO 512 MHz FROM MASTER OSCILLATOR A1
A2P1 (MATES WITH A1A1J1)
BAND 1 AMPLIFIER BOARD A2A1
L6
R8 10K
SWITCH Q4 2N5183
SENSING AMPLIFIER Q3 2N5133
C19 180 PF
C20 270 PF
C12 0.001
SATURATED BUFFER AMPLIFIER
C9 0.001
R9 47
C13 0.001
R16 330
R15 10
L5
C17 0.001
C18 0.01
R17 150
R4 300
L3
Q5 2N5179
T1
C2 0.001
C1 1PF
R1 75
C5 2PF
L1
Q1 2N5179
C8 0.001
C10 15PF
R10 100
R11 330
R13 330
C14 0.01
C15 0.001
R12 47
R6 47
R7 300
C11 0.001
C16 0.001
R18 150
L1
R2 620
C3 0.001
R3 510
C4 6PF
ISOLATION AMPLIFIER Q2 A473
R5 47
C6 0.01
C7 0.001
RANGE MHz
S1
A2J1
DIVIDED OUTPUT TO A3A2P1
NOTES
UNLESS OTHERWISE SPECIFIED
1 ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 WATT
2 ALL CAPACITOR VALUES ARE IN MICROFARADS
3 RANGE MHz SWITCH SHOWN IN 248-512 POSITION
4 * INDICATES FACTORY SELECT COMPONENT NOMINAL VALUE SHOWN
9 Q1 & Q2 MATCHED PAIRS
FL1 0.005
L1
R2 1K
C3 0.001
R1 1K
C2 0.001
BAND 2,3 & 4 FREQUENCY DIVIDER ASSY A2A2
BAND 2 FREQUENCY DIVIDER BOARD A2A2A1
R1 1K
C2 10PF
CR1 FDH666
R18 100
C1 15PF
L1
C3 15PF
R19 200
R2 91
C4 56PF
Q1 2N5179 9
R3 150
C7 6.8PF
R5 2K 1/8W
C6 0.001
C8 0.001
R4 300
C5 68PF
CR2
CR3
R6 330
C9 6.8PF
R7 2K 1/8W
R8 150
C10 68PF
R9 300
Q2 2N5179 9
R11 10
R10 120
C11 0.001
R12 5.6K
R13 1K
R15 560
L3
Q3 A473
R14 220
C14 39PF
C12 0.01
C13 6PF
L2
R16 150
C15 33PF
Q4 2N4917
R17 200
ISOLATION AMPLIFIER
BINARY DIVIDER
C4 0.001
FL2 0.005
C7 0.001
L2
BAND 3 FREQUENCY
R1 1K
C3 22PF
CR1 FDH666
R19 100
C2 43PF
L1
R3 * 100
R4 * 220
R5 * 1K
A2A3A1 P/O
R16, 1.5K *
R19 * 820
2
3
4
5
6
7
8



6-3

Figure 6-3. Frequency Divider Assembly A2, Schematic Diagram (Sheet 1 of 2).

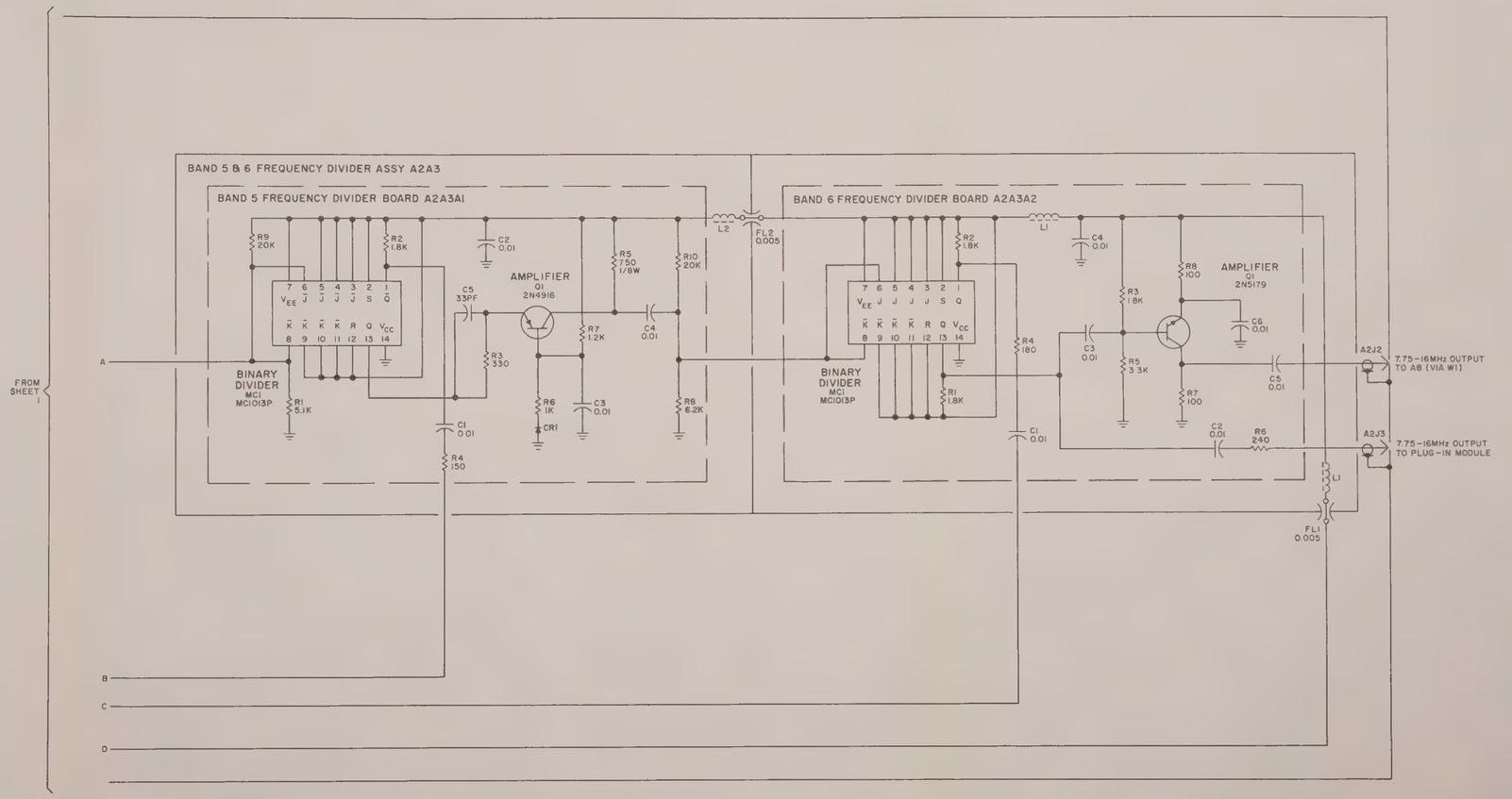
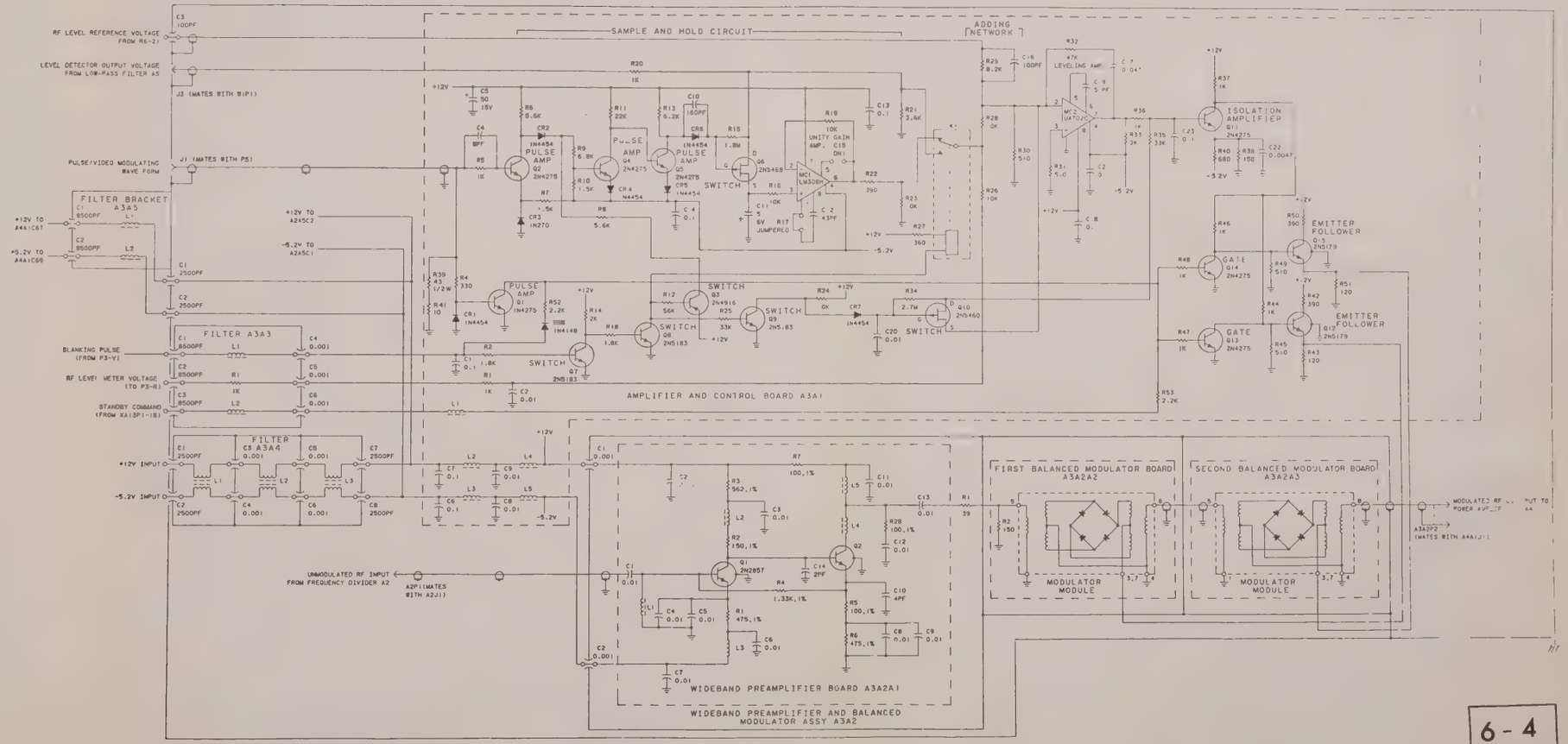


Figure 6-3. Frequency Divider Assembly A2, Schematic Diagram (Sheet 2 of 2).

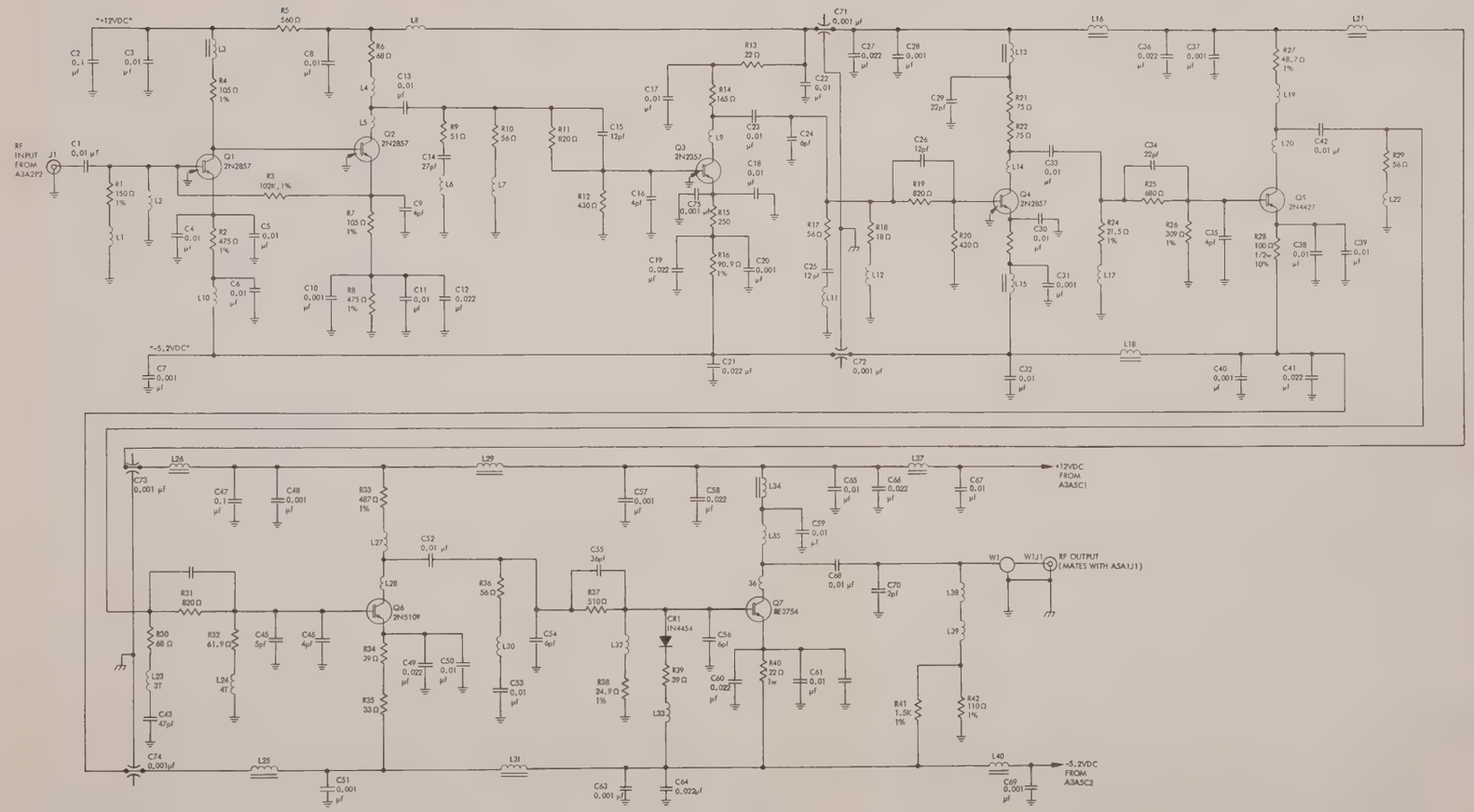
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W
2. ALL CAPACITOR VALUES ARE IN MICROFARADS



6-4

Figure 6-4. Balanced Modulators and Level Control A3, Schematic Diagram. 6-11/6-12



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS 1/4w, 5%.

6-5

Figure 6-5. Power Amplifier, 5Ω, 520 MHz, A4A1, Schematic Diagram.

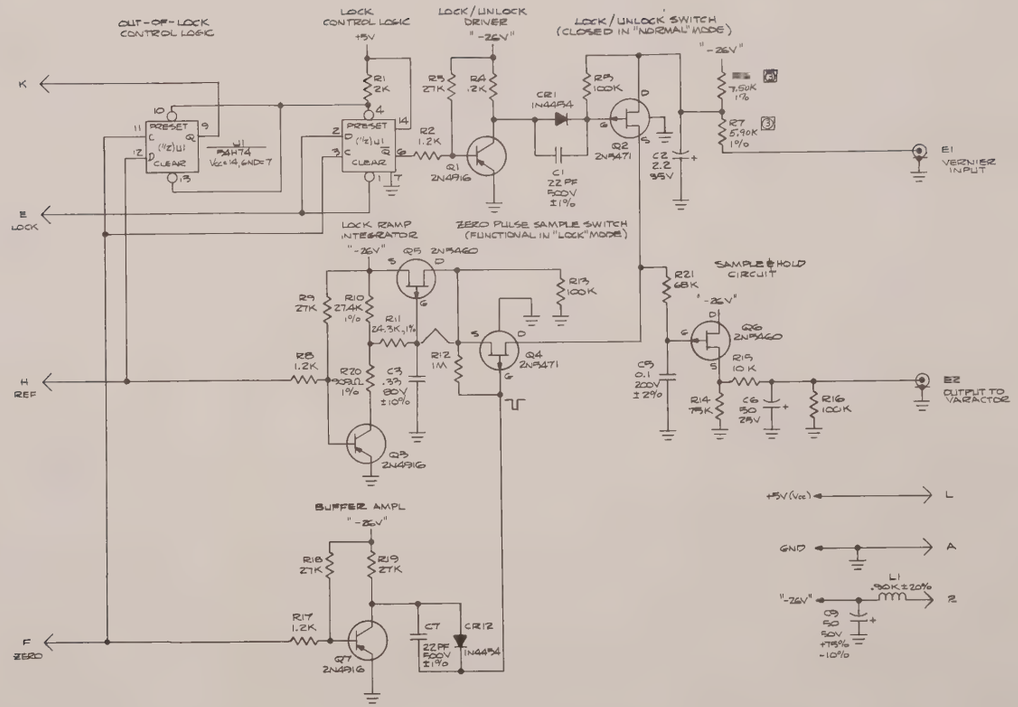
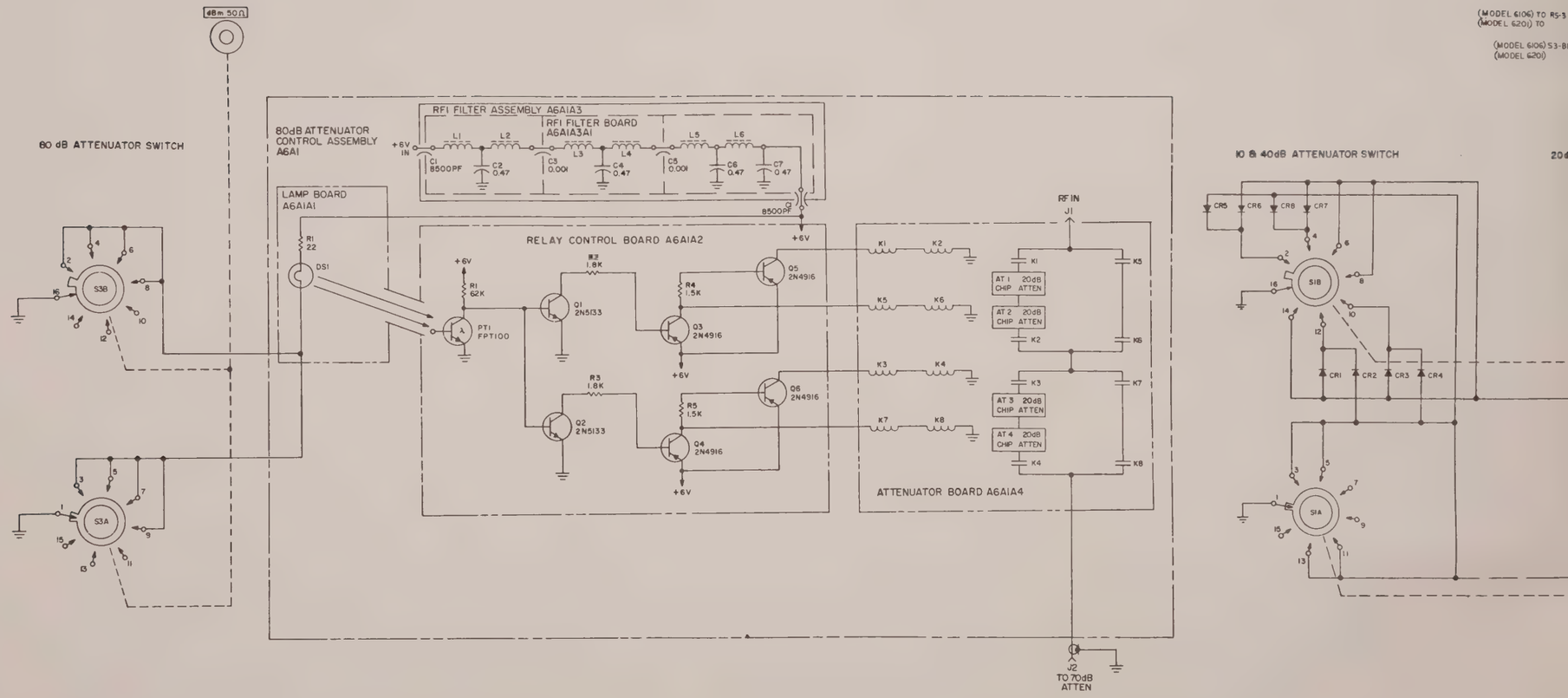
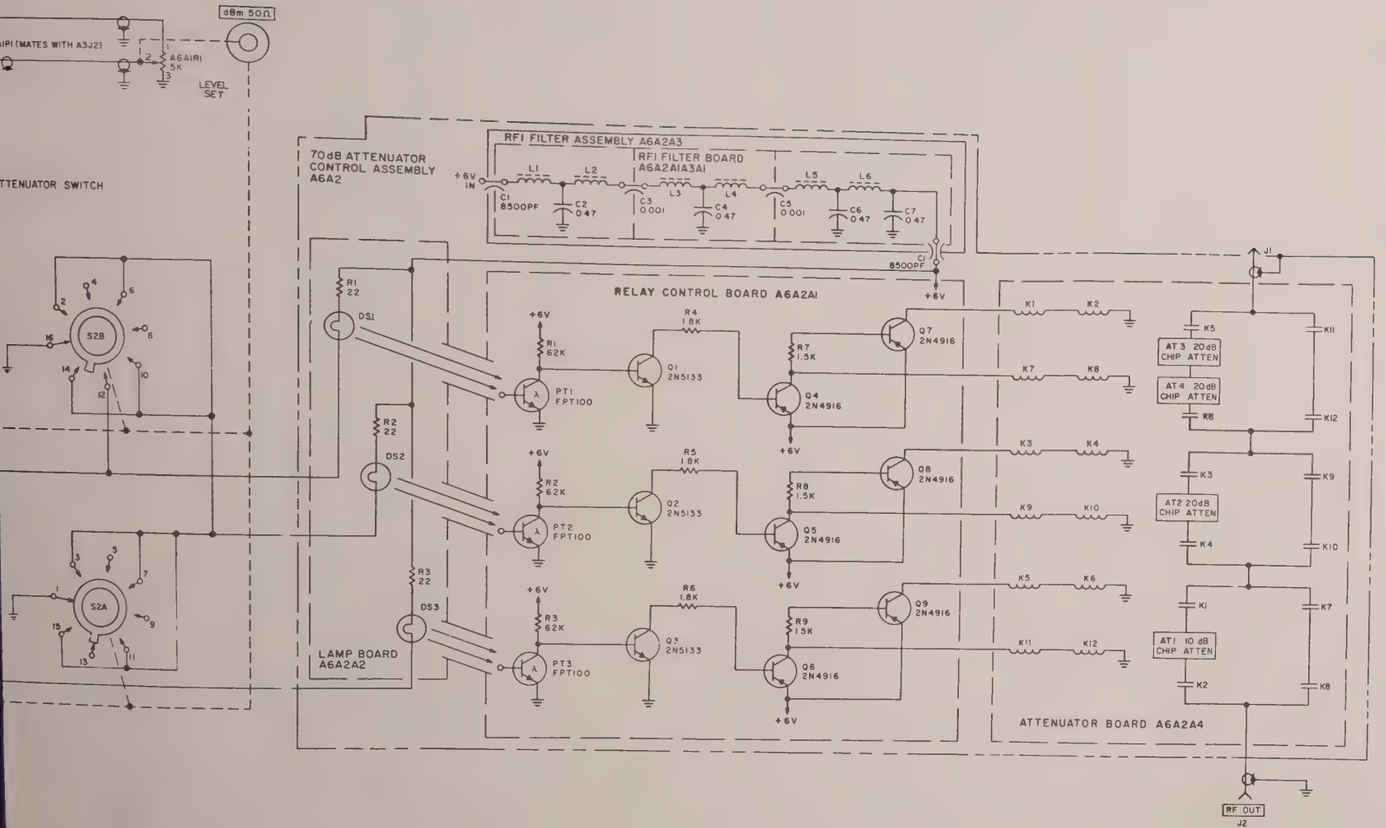


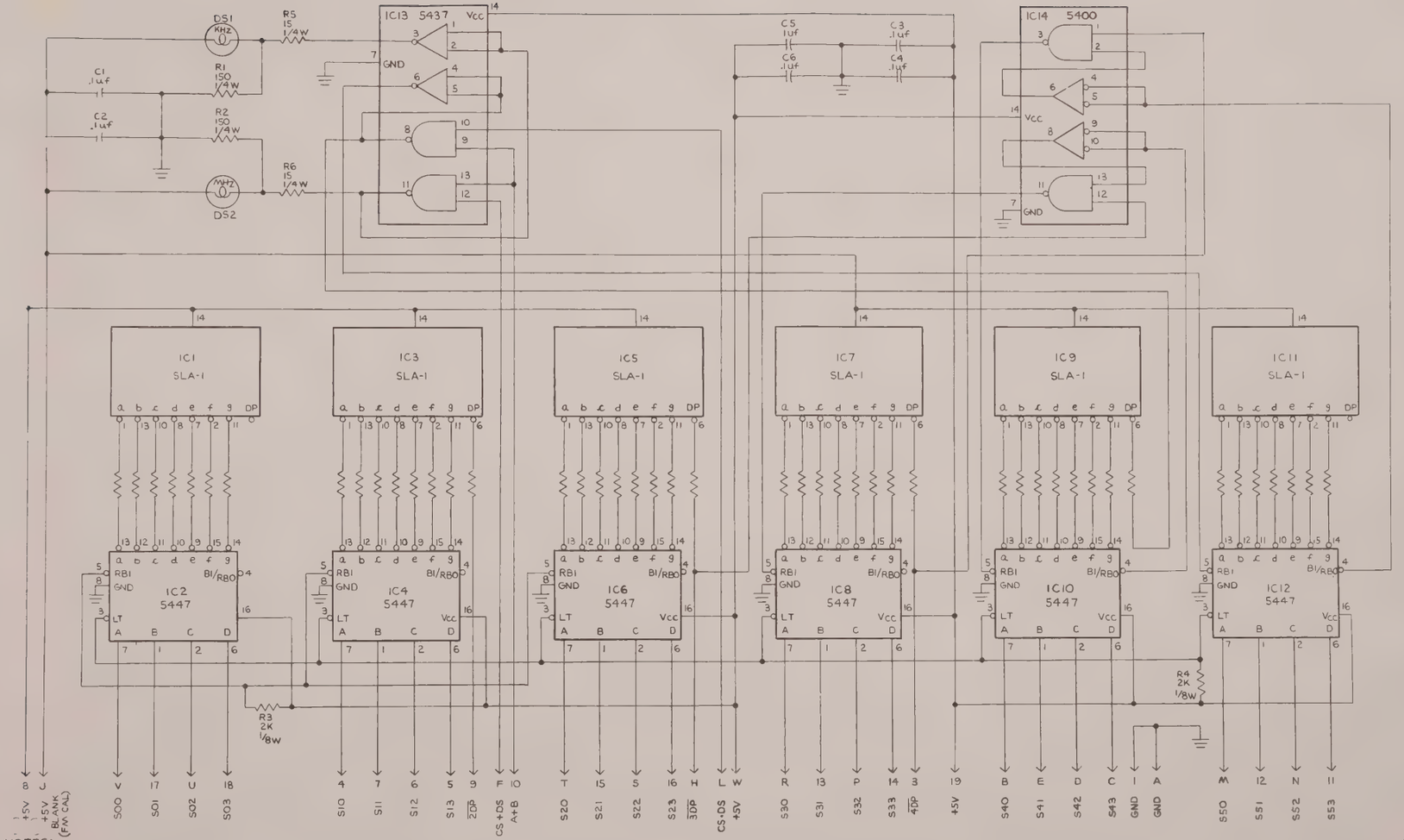
Figure 6-6. Amplifier Frequency Counter A8A3A7, Schematic Diagram.


48m 50Ω
80 dB ATTENUATOR SWITCH
80dB ATTENUATOR CONTROL ASSEMBLY A6A1
RFI FILTER ASSEMBLY A6A1A3
RFI FILTER BOARD A6A1A3A1
+6V IN
L1
L2
L3
L4
L5
L6
C1 8500PF
C2 0.47
C3 0.001
C4 0.47
C5 0.001
C6 0.47
C7 0.47
C8 8500PF
LAMP BOARD A6A1A1
R1 22
DS1
RELAY CONTROL BOARD A6A1A2
+6V
R2 62K
PT1 FPT100
R3 1.8K
Q1 2N5133
R4 1.5K
Q3 2N4916
Q5 2N4916
R3 1.8K
Q2 2N5133
R5 1.5K
Q4 2N4916
Q6 2N4916
K1
K2
K3
K4
K5
K6
K7
K8
RF IN
J1
AT 1 20dB CHIP ATTEN
AT 2 20dB CHIP ATTEN
AT 3 20dB CHIP ATTEN
AT 4 20dB CHIP ATTEN
ATTENUATOR BOARD A6A1A4
J2
TO 70dB ATTEN
S3A
S3B
10 & 40dB ATTENUATOR SWITCH
S1A
S1B
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8



NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4WATT
2. ALL CAPACITOR VALUES ARE IN MICROFARADS
3. dBm 50Ω SWITCH SHOWN IN 20 22V POSITION VIEWED FROM FRONT PANEL END OF SHAFT
4. ALL DIODES ARE TYPE IN4454

Figure 6-7. RF Attenuator A6, Schematic Diagram.



NOTES:

1. UNLESS OTHERWISE NOTED ALL RESISTORS ARE 200 Ω, 1/8W, 5%
2. UNLESS OTHERWISE NOTED ALL CAPACITORS ARE 25V ±20%
3. ALL VOLTAGES ARE DIMMER CONTROLLED
4. MODEL 6201 SPEC 1903 (NAFI)

Figure 6-8. Display Board A8A3A2, Schematic Diagram.

NOTES: UNLESS OTHERWISE NOTED.
1. ALL RES ARE IN Ω, 1/4W, 5%.
2. ALL CAPACITORS ARE 25V, ± 20%.

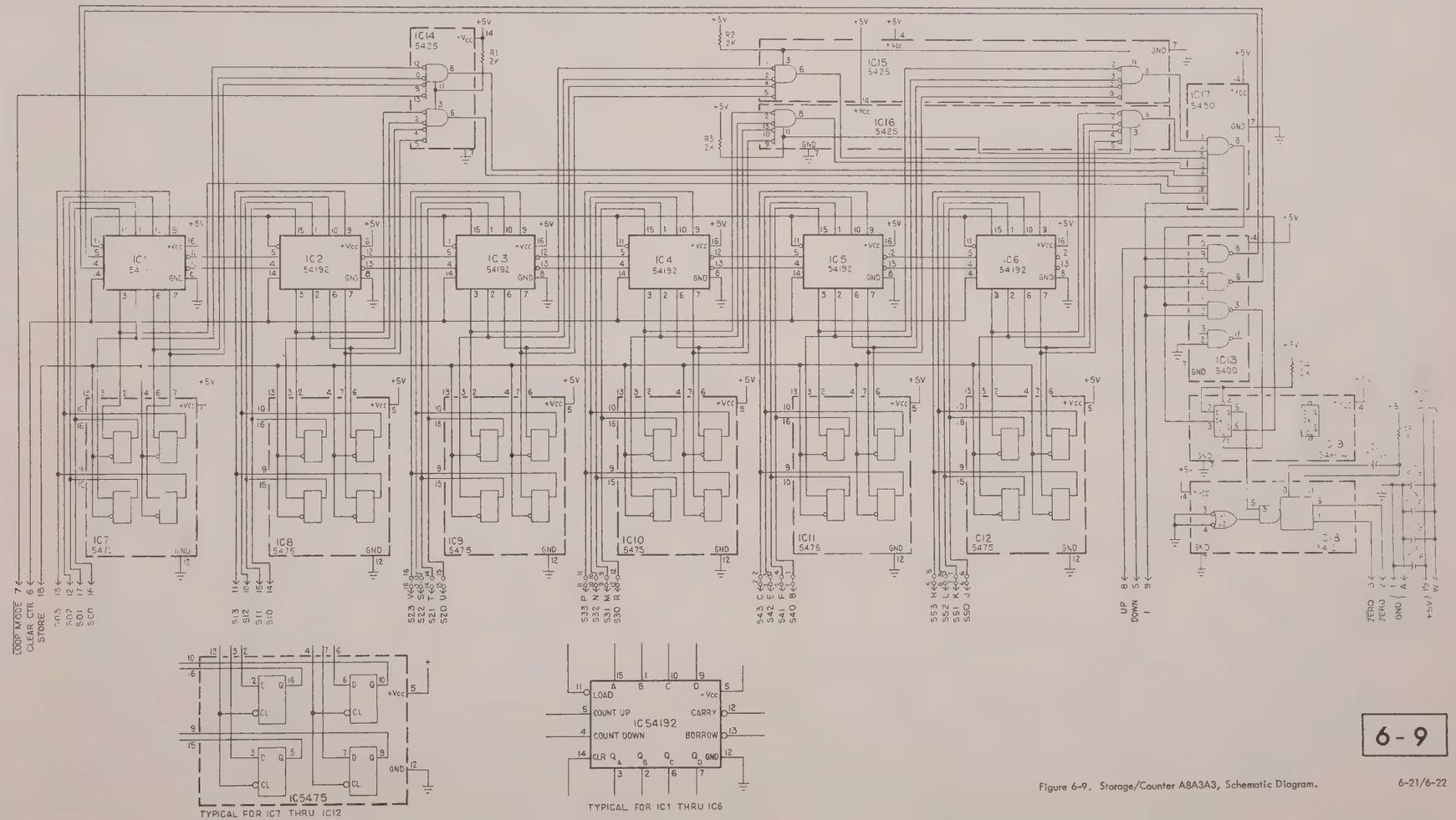
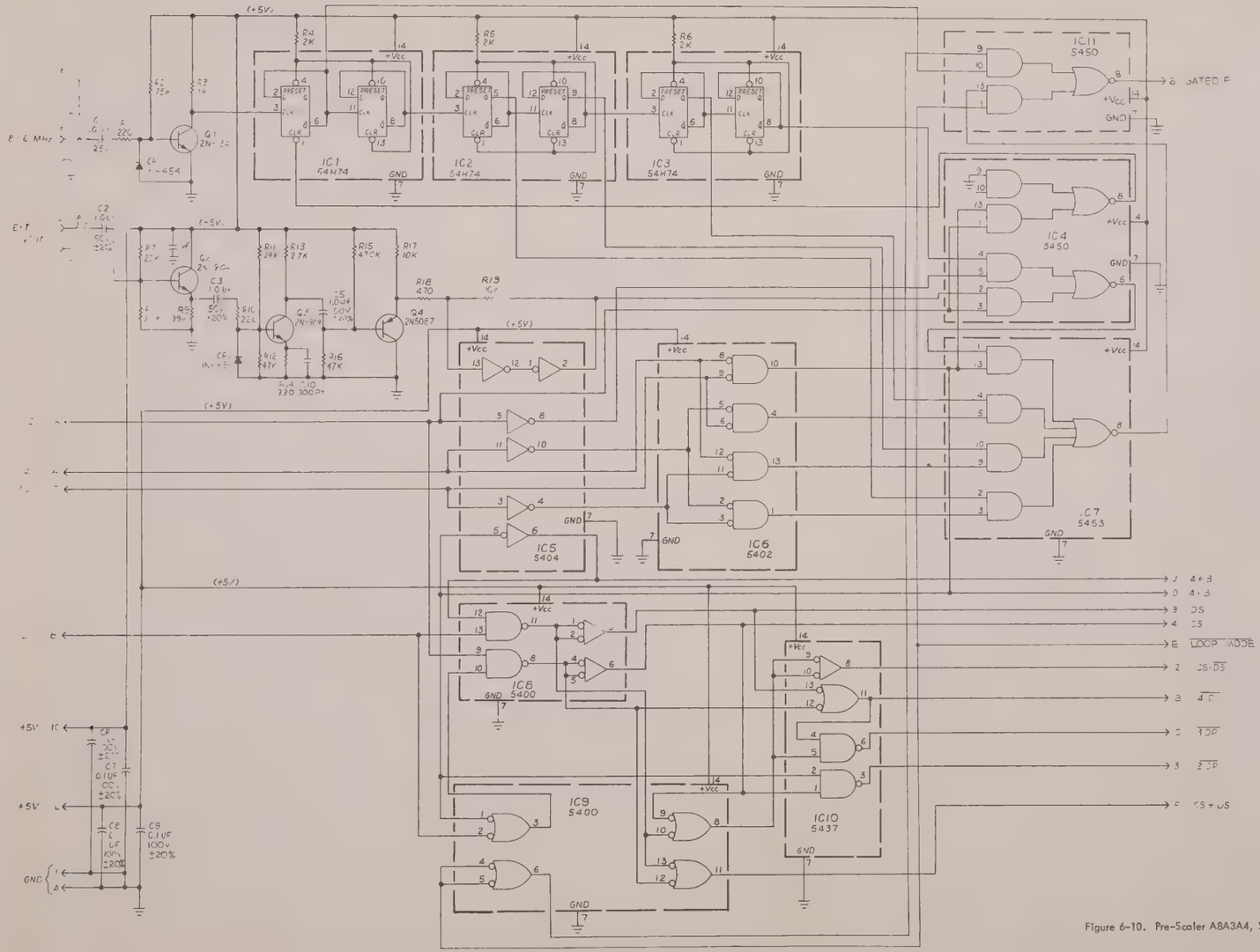


Figure 6-9. Storage/Counter A8A3A3, Schematic Diagram.

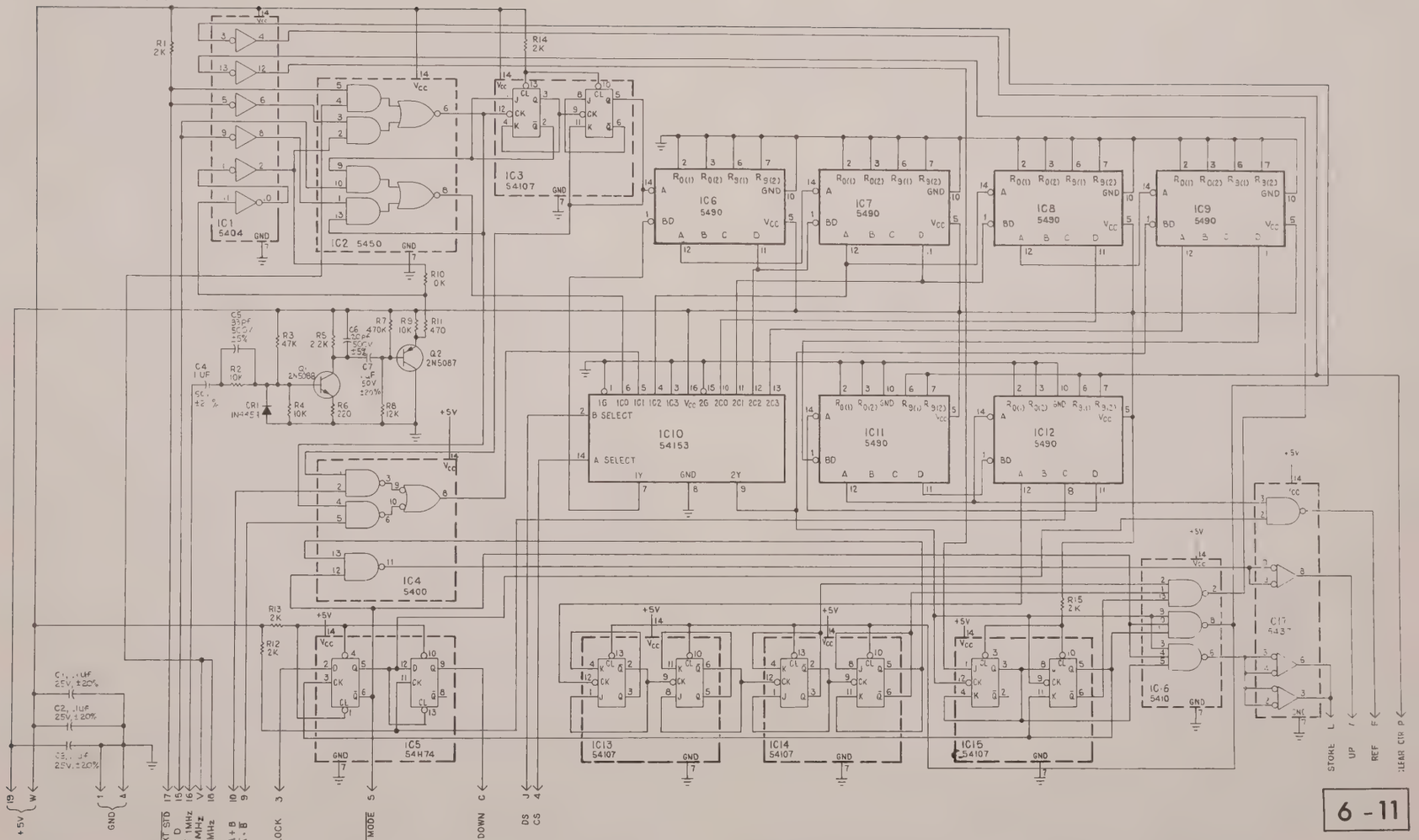
6-21/6-22



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS IN OHMS, 1/4W, 5%

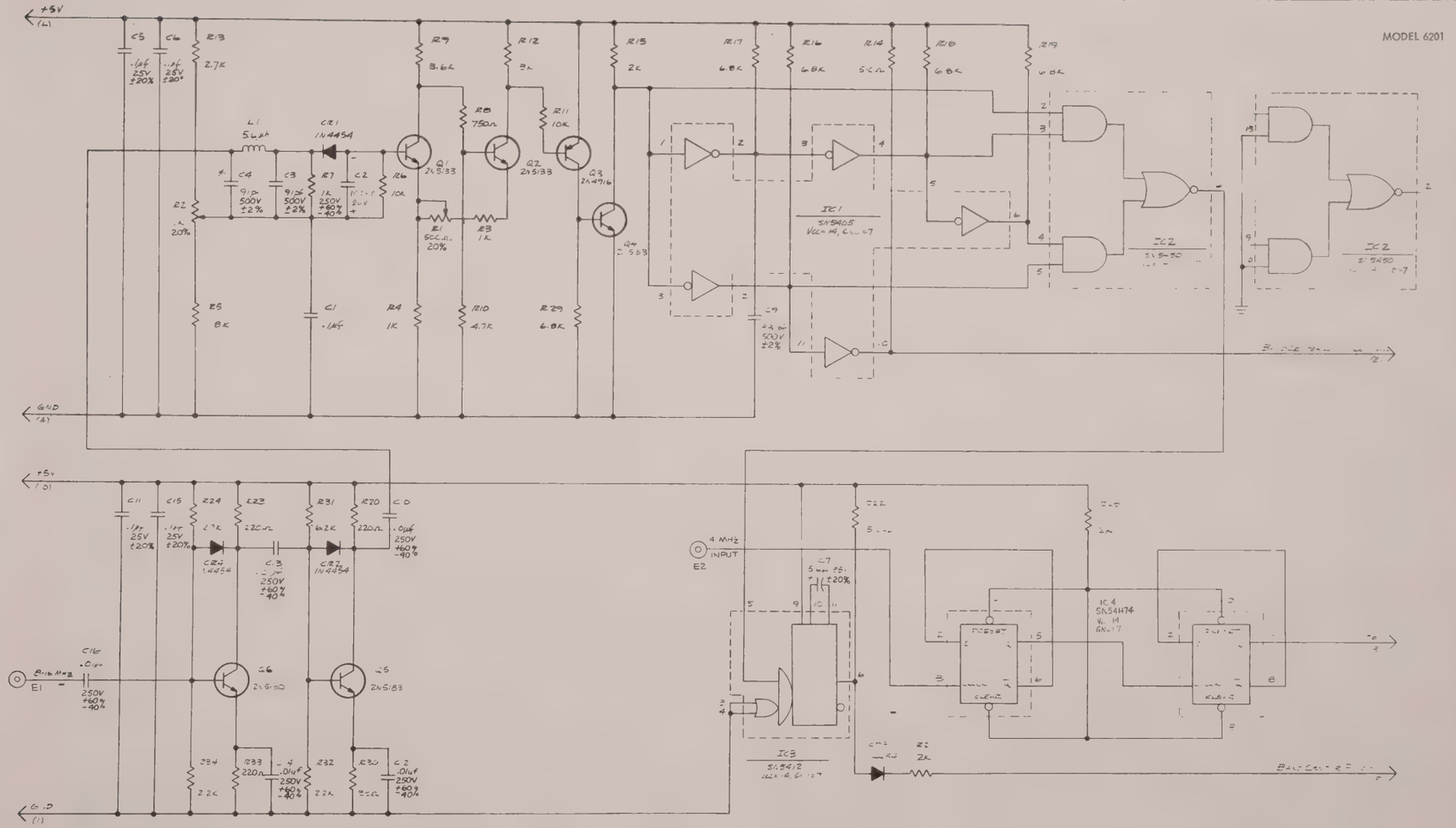
Figure 6-10. Pre-Scaler A8A3A4, Schematic Diagram.

NOTES: UNLESS OTHERWISE NOTED.
1. ALL RES ARE IN Ω, ¼W, 5%.



6 - 11

Figure 6-11. Time Base A8A3A5, Schematic Diagram.



* FACT. SELECT, NOMINAL VALUE SHOWN
1- ALL RESISTORS 1/4W, 5% CARBON
NOTES: UNLESS SPECIFIED OTHERWISE:

Figure 6-12. Oscillator PC Board A8A3A6, Schematic Diagram.

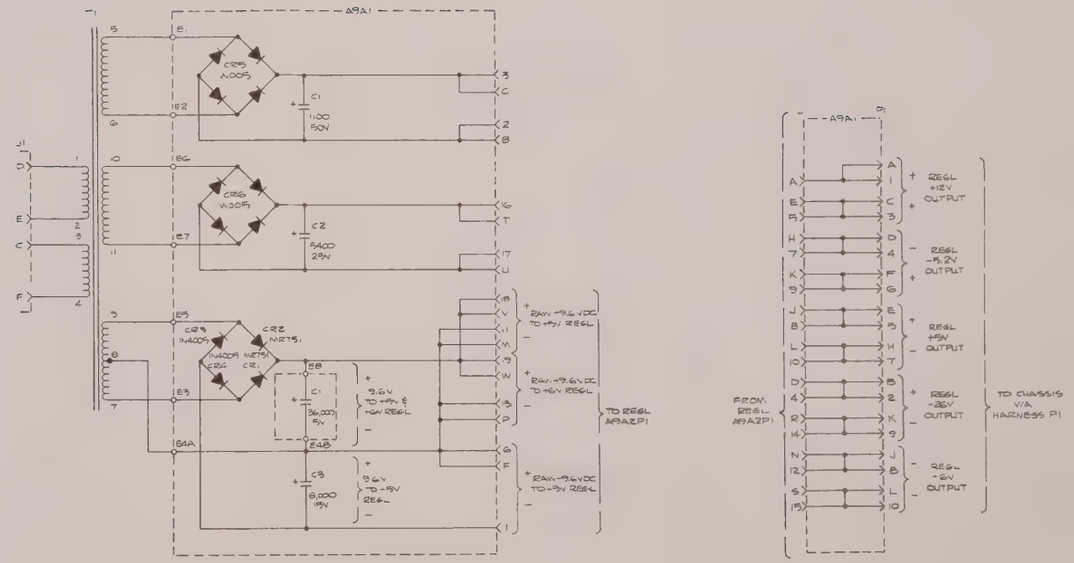
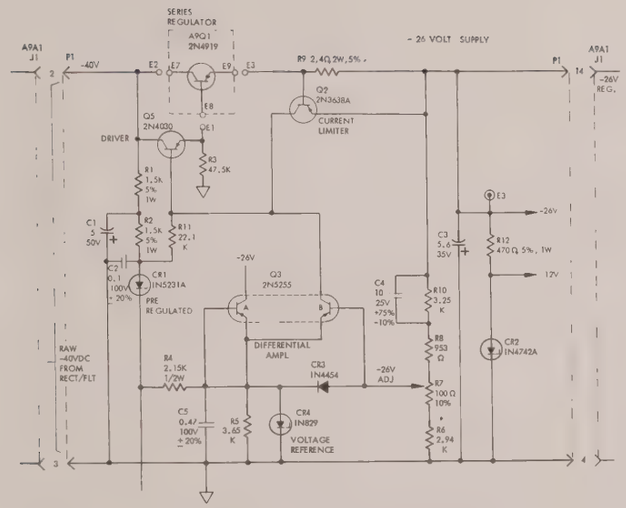
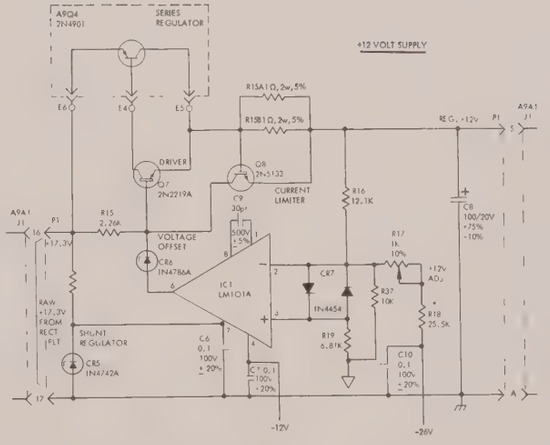
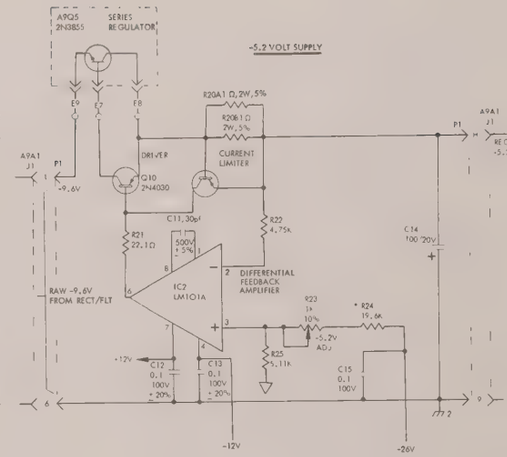
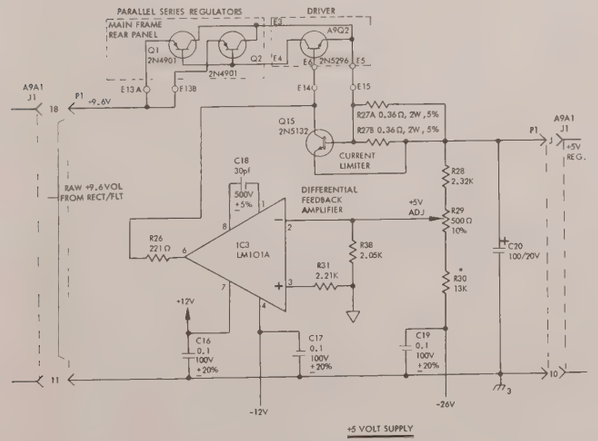


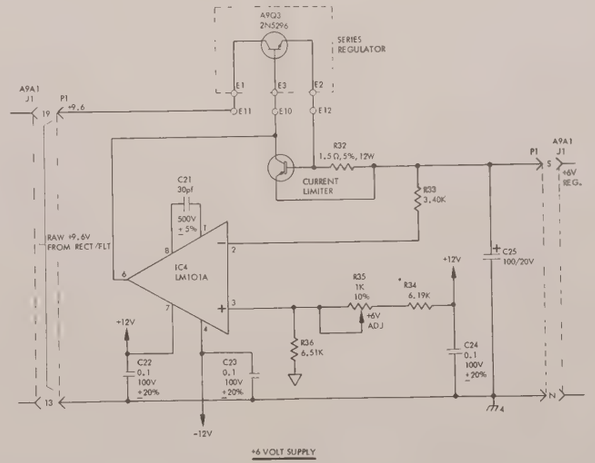
Figure 6-13. Power Supply A9A1, Schematic Diagram.











NOTES: UNLESS OTHERWISE SPECIFIED.

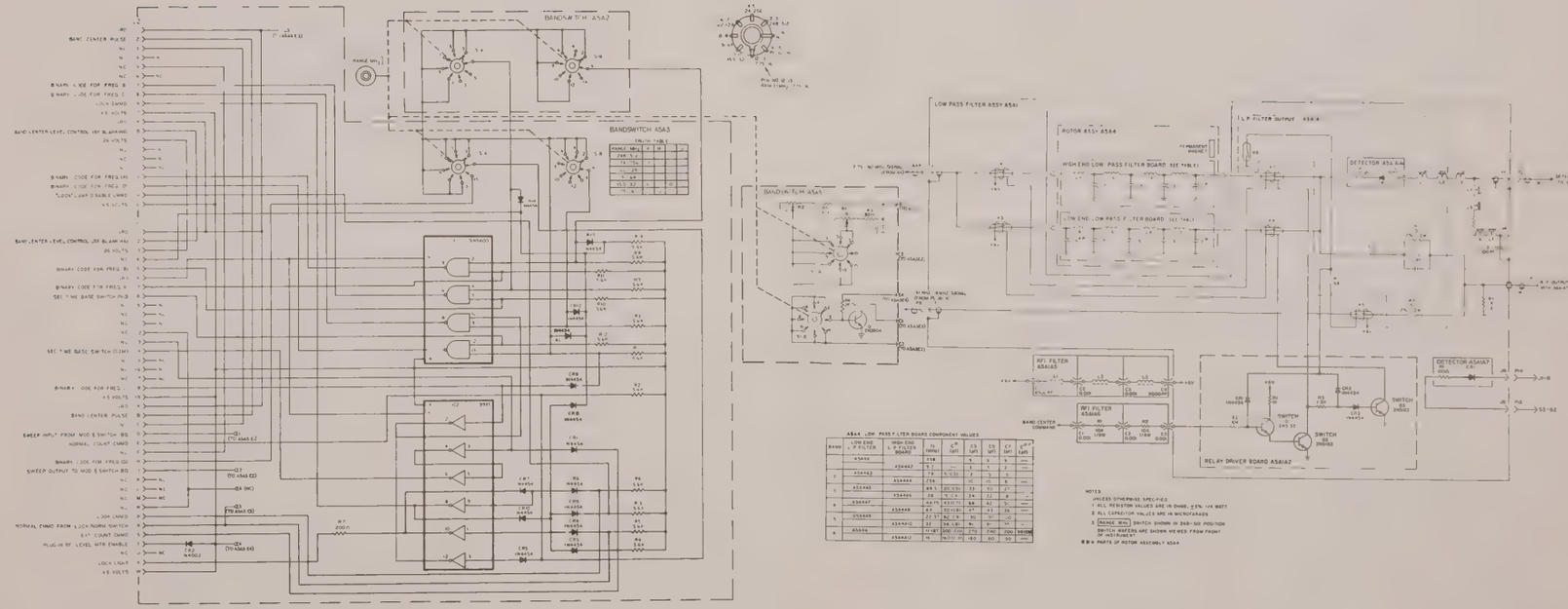
1. * INDICATES FACTORY SELECTED COMPONENT.
2. ALL CAPACITORS IN μf.
3. ALL RESISTORS 1/4w, 1%.
4. ⏚ 1, 2, 3, 4 ARE CONNECTED TO REF END ▽ AND CHASSIS END ⏚ WITHIN THE CHASSIS WIRING EXTERNAL TO THIS MODULE.
5.

FIRST USED	LAST USED	UNUSED
R1	R38	R11
C1	C25	
Q2	Q17	Q1, 4, 6, 9, 12-14, 16
IC1	IC4	
CR1	C88	

6. "E" - NUMBERED TERMINALS SHOWN ON SMALL DOTTED INSETS ARE RCB A9A3. TRANSISTORS A9Q1 - A9Q3 SHOWN THEREON ARE MOUNTED TO THE POWER SUPPLY MOSULE AND CONNECTED TO A9A3. ALL OTHER "E" NUMBERED TERMINALS ARE ON THE A9A2 P.C.B.

6-14

Figure 6-14. Power Supply A9A2 and A9A3, Schematic Diagram.



A5A4 LOW PASS FILTER BOARD COMPONENT VALUES

BAND	LOW END L.P. FILTER	HIGH END L.P. FILTER BOARD	L1 (MHz)	C8 (pF)	C9 (pF)	C5 (pF)	C7 (pF)	C6** (pF)
1	A5A1A2		118		8	4	4	—
		A5A4A2	5	—	3	1	2	—
	A5A1A3		18	8.2 (3)	5	3	3	—
2		A5A4A4	7.96		12	5	5	—
	A5A1A4		49.5	22 (3)	24	10	27	—
		A5A4A6	29	8.2	24	12	8	—
3	A5A1A5		44.75	43 (1)	68	62	51	—
		A5A4A8	69	22 (1)	47	43	39	—
4	A5A1A6		27.37	62 (1)	30	30	20	—
		A5A4A10	32	56 (1)	24	30	24	—
5	A5A1A7		11.487	200 (1)	170	140	200	200 (3)
		A5A4A12	16	160 (1)	120	80	50	—

NOTES
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS, ±5% 1/4 WATT
2. ALL CAPACITOR VALUES ARE IN MICROFARADS
3. RANGE MHz SWITCH SHOWN IN 260-320 POSITION
SWITCH WAFERS ARE SHOWN VIEWED FROM FRONT OF INSTRUMENT
** P/O PARTS OF MOTOR ASSEMBLY A5A4

Figure 6-15. Low Pass Filter A5, Schematic Diagram.

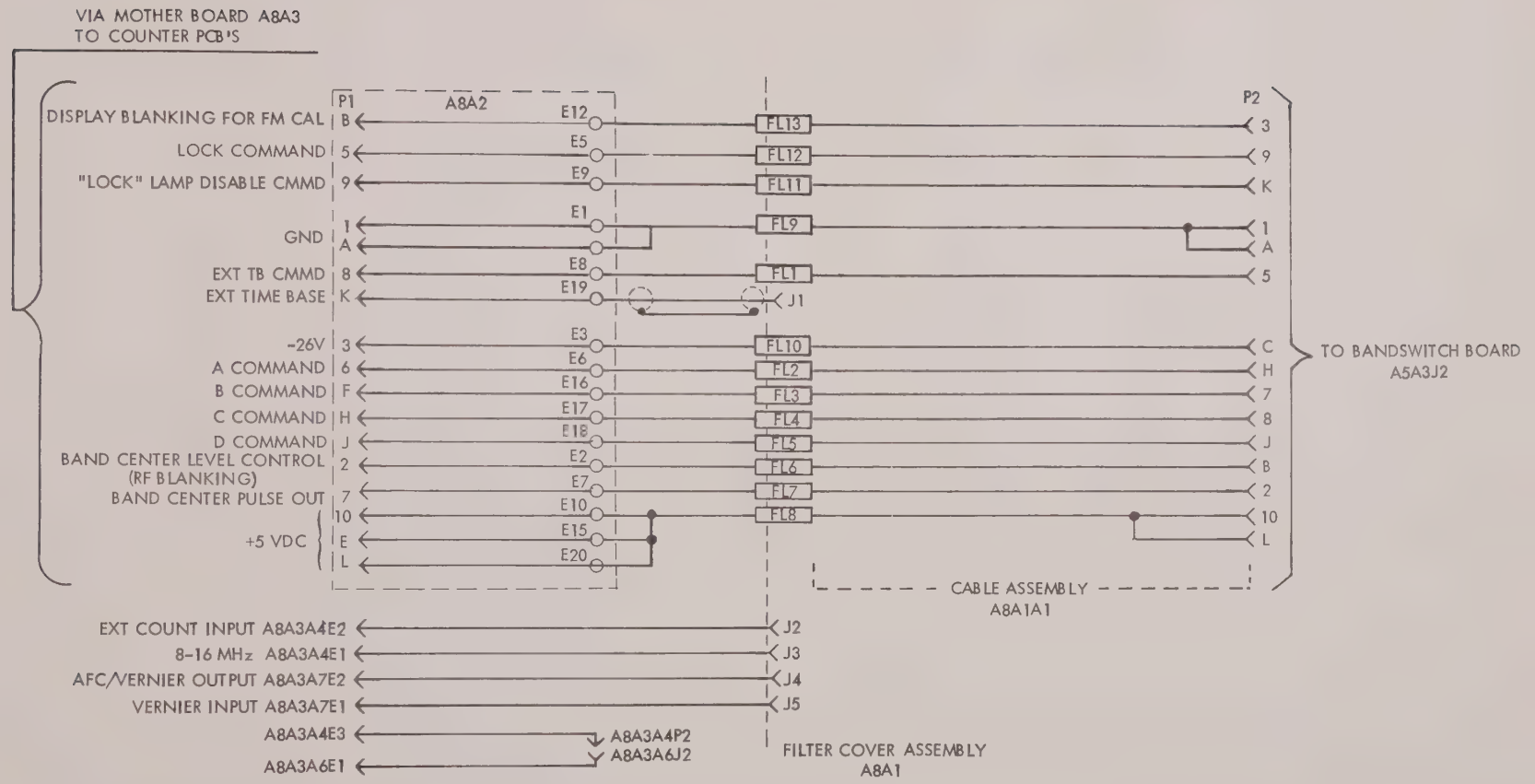


Figure 6-16. Pushbutton and Modulation PC Board A7, Schematic Diagram.

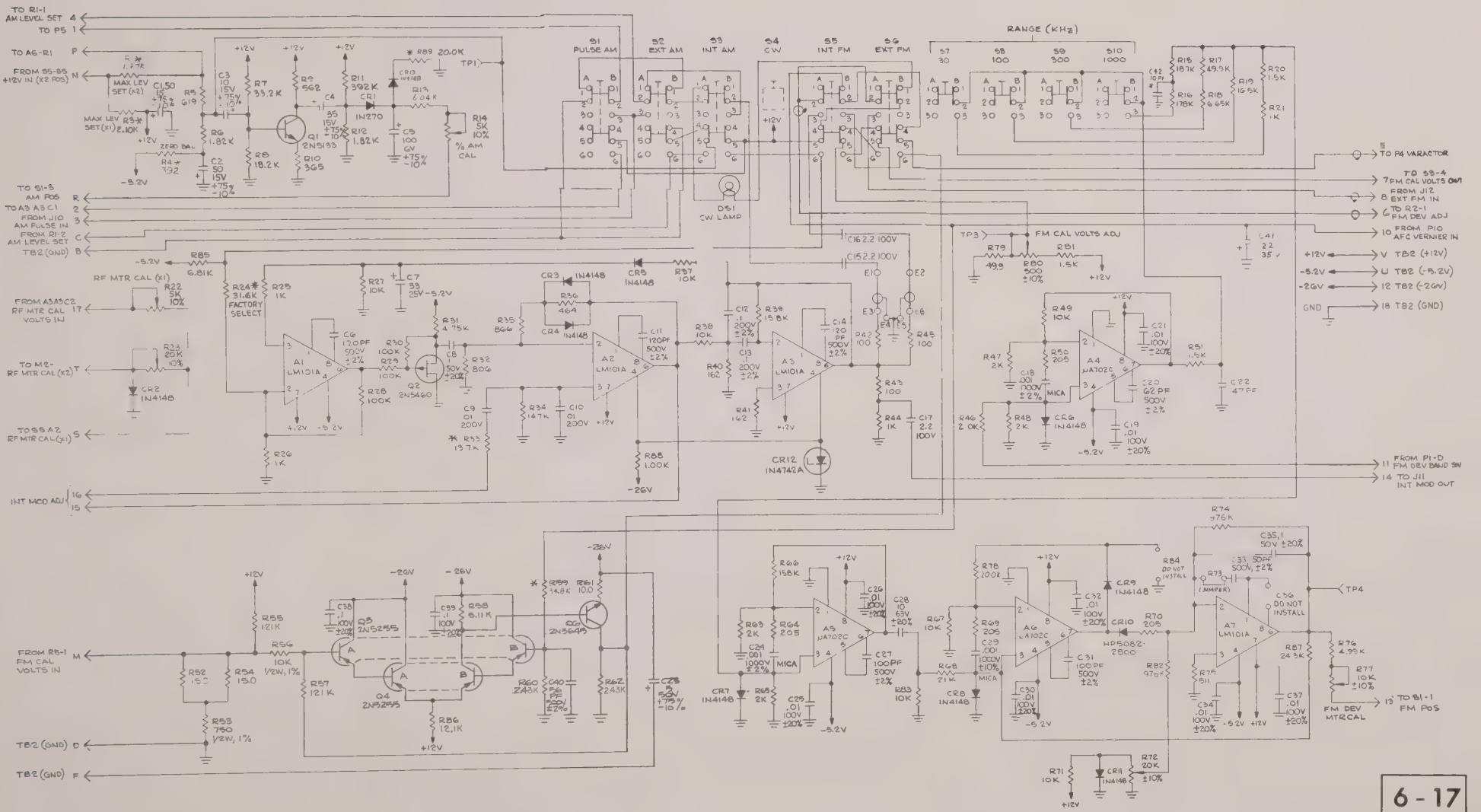


Figure 6-17. Counter Interconnect, Schematic Diagram.

6-37/6-38

DISPLAY J2

1	GND	A	GND
2	J1-B K1-1	B	J3-B
3	J4-B	C	J3-C
4	J3-14	D	J3-E
5	J3-11	E	J3-F
6	J3-10	F	J4-E
7	J3-15	H	J4-C
8	+5V J1-E	J	K1-2
9	J4-3	K	—
10	J4-J	L	J4-2
11	J3-H	M	J3-J
12	J3-K	N	J3-L
13	J3-M	P	J3-N
14	J3-P	R	J3-R
15	J3-T	S	J3-S
16	J3-V	T	J3-U
17	J3-17	U	J3-12
18	J3-13	V	J3-16
19	+5V	W	+5V

STORAGE/ COUNTER J3

1	GND	A	GND
2	J7-F	B	J2-B
3	J7-D	C	J2-C
4	—	D	—
5	J5-C	E	J2-D
6	J5-P	F	J2-E
7	J5-5	H	J2-11
8	J5-7	J	J2-M
9	J4-6	K	J2-12
10	J2-6	L	J2-N
11	J2-5	M	J2-13
12	J2-U	N	J2-P
13	J2-18	P	J2-14
14	J2-4	R	J2-R
15	J2-7	S	J2-S
16	J2-V	T	J2-15
17	J2-17	U	J2-T
18	J5-L	V	J2-16
19	+5V	W	+5V

PRE-SCALER J4

1	GND	A	GND
2	J2-L	B	J2-3
3	J2-9	C	J2-H
4	J5-4	D	J5-9
5	—	E	—
6	J3-9	F	J2-F
7	J1-F	H	J1-6
8	J5-15	J	J2-10 J5-10
9	J5-J	K	J1-H
10	+5V	L	+5V

TIME/BASE J5

1	GND	A	GND
2	—	B	—
3	J7-E	C	J3-5
4	J4-4	D	—
5	J3-7	E	—
6	—	F	J7-H
7	J3-8	H	—
8	—	J	J4-9
9	J4-D	K	—
10	J4-J	L	J3-18
11	—	M	—
12	—	N	—
13	—	P	J3-6
14	—	R	—
15	J4-8 J1-J	S	—
16	J1-K	T	—
17	J1-8	U	—
18	J6-3	V	—
19	+5V	W	+5V

OSCILLATOR J6

1	GND	A	GND
2	J1-2	B	—
3	J5-18	C	—
4	—	D	—
5	J1-7	E	—
6	—	F	—
7	—	H	—
8	—	J	—
9	—	K	—
10	+5V	L	+5V

AFC J7

1	GND	A	GND
2	J1-3	B	—
3	—	C	—
4	—	D	J3-3
5	—	E	J5-3 J1-5
6	—	F	J3-2
7	—	H	J5-F
8	—	J	—
9	—	K	J1-9
10	+5V	L	+5V

OUTPUT J1

1	GND	A	GND
2	J6-2	B	J2-2
3	J7-2	C	—
4	—	D	—
5	J7-E	E	+5V TZ-8 only
6	J4-H	F	J4-7
7	J6-5	H	J4-K
8	J5-17	J	J5-15
9	J7-K	K	J5-16
10	+5V	L	+5V

1	GND	A	GND
2	BAND MTR LEVEL CONTROL	B	
3	-26V	C	
+		D	
5	LOCK	E	+5V
6	'A'	F	'B'
7	BAND CNTR PULSE	H	'C'
8	EXT STD	J	'D'
9	NORMAL	K	EXT 1 MHZ
10	+5V	L	+5V

NOTE:
1. ON 6201 SPEC 1903 ONLY +5V SUPPLIED TO J1-E ONLY IS DIMMER CONTROLLED

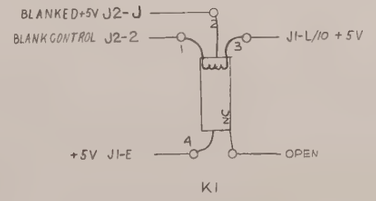


Figure 6-18. Mother Board Interconnect A8A3, Schematic Diagram.

SHIPMENT DAMAGE CLAIM

The instrument should be tested as soon as it is received. If it fails to operate properly or is damaged in any way, a claim must be filed with the carrier. Have carrier agent inspect damage to instrument and packing crate and forward us a copy of his written report. You will then be advised of replacement or repair arrangements and disposition of the equipment. Please include model number, type number and serial number when referring to this instrument for any reason.

REPACKING FOR SHIPMENT

The instrument should be packed in the original carton. If unusable or not available, use a wooden box with approximately three inches of excelsior or other shock-absorbing material surrounding the instrument. If desired, packing services of a local transfer and storage company may be employed.

SINGER
INSTRUMENTATION

CHAMPION CLASP NO. 55
6 x 9

MP MASTER
MA30333